

Features

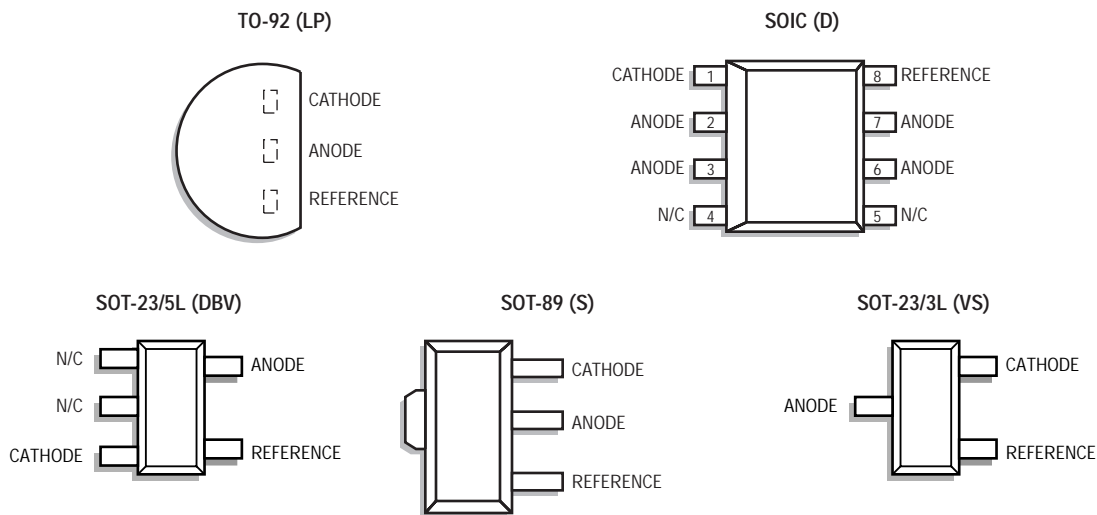
- Temperature-compensated: 50 ppm/°C
- 0.25% to 2.0% bandgap offered
- Internal amplifier with 100 mA capability
- Multiple temperature ranges
- Low frequency dynamic output impedance: < 150 mΩ
- Low output noise

Description

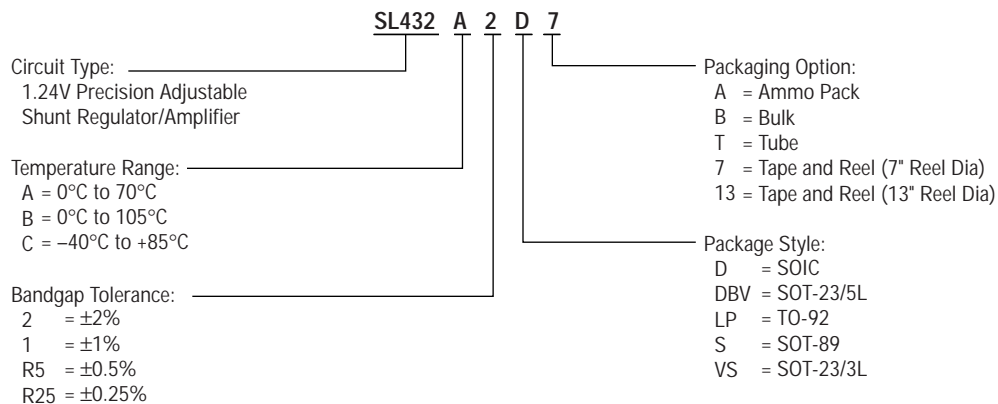
The SL432 is a three terminal adjustable shunt regulator utilizing an accurate 1.24V bandgap reference. The SL432 is functionally similar to an AS431 except for its lower reference voltage, making it usable in a wide variety of low voltage applications.

Because of its robust bipolar technology, the SL432 handles a wide range of current, and holds off more than 18V so its use is not limited to low power, low voltage systems. Significant care has been taken to provide adequate AC bandwidth to allow the SL432 as an amplifier in control systems and power electronics.

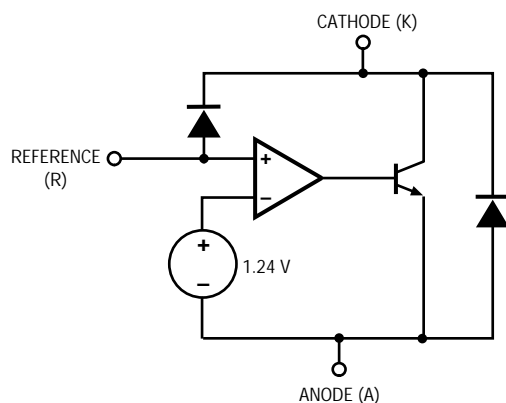
Pin Configuration — Top view



Ordering Information



Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	18	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	100	mA
Reference Input Current	I_{REF}	1	mA
Continuous Power at 25°C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
SOT-23/3L/5L		200	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 18	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160°C/W	80°C/W	6.3 mW/°C
SOIC	175°C/W	45°C/W	5.7 mW/°C
SOT-89	110°C/W	8°C/W	9.1 mW/°C
SOT-23/3L/5L	575°C/W	150°C/W	1.7 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over the full junction temperature range (0–105°C). Ambient temperature must be derated based upon power dissipation and package thermal characteristics. Unless otherwise stated, test conditions are: $V_{KA} = V_{REF}$ and $I_K = 10$ mA.

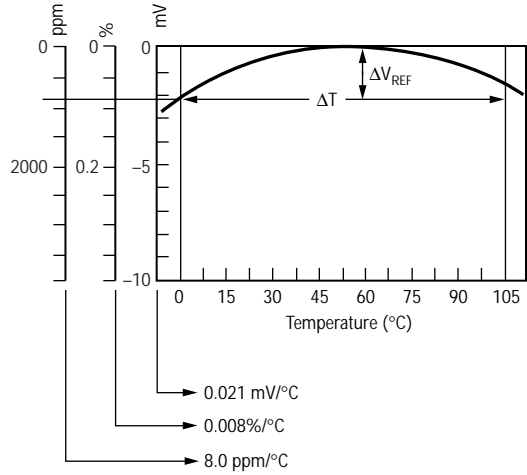
Parameter	Symbol	Test Condition	SL432 (0.25%)			SL432 (0.5%)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	V_{REF}	$I_K = 10$ mA $T_J = 25^\circ\text{C}$ $V_K = V_{REF}$	1.237	1.240	1.243	1.234	1.240	1.246	V
Line Regulation	ΔV_{REF}	$V_{KA} = 1.25$ to 15 V		28	50		28	50	mV
Load Regulation	ΔV_{REF}	$I_K = 1$ to 100 mA		3.9	6		3.9	6	mV
Temperature Deviation	ΔV_{REF}	$0 < T_J < 105^\circ\text{C}$		5	10		5	10	mV
Reference Input Current	I_{REF}			2.3	6		2.3	6	μA
Reference Input Current Temperature Coefficient	ΔI_{REF}	$0 < T_J < 105^\circ\text{C}$		0.14	0.6		0.14	0.6	μA
Minimum Cathode Current for Regulation	$I_{K(\min)}$			0.2	1		0.2	1	mA
Off State Leakage	$I_{K(\min)}$	$V_{REF} = 0$ V, $V_{KA} = 15$ V		0.04	500		0.04	500	nA

Parameter	Symbol	Test Condition	SL432 (1.0%)			SL432 (2.0%)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	V_{REF}	$I_K = 10$ mA $T_J = 25^\circ\text{C}$ $V_K = V_{REF}$	1.228	1.240	1.252	1.215	1.240	1.256	V
Line Regulation	ΔV_{REF}	$V_{KA} = 1.25$ to 15 V		28	50		28	50	mV
Load Regulation	ΔV_{REF}	$I_K = 1$ to 100 mA		3.9	6		3.9	6	mV
Temperature Deviation	ΔV_{REF}	$0 < T_J < 105^\circ\text{C}$		5	12		5	12	mV
Reference Input Current	I_{REF}			2.3	6		2.3	6	μA
Reference Input Current Temperature Coefficient	ΔI_{REF}	$0 < T_J < 105^\circ\text{C}$		0.14	0.6		0.14	0.6	μA
Minimum Cathode Current for Regulation	$I_{K(\min)}$			0.2	1		0.2	1	mA
Off State Leakage	$I_{K(\min)}$	$V_{REF} = 0$ V, $V_{KA} = 15$ V		0.04	500		0.04	500	nA

*Temperature deviation is defined as the maximum deviation of the reference over the given temperature range and does not imply an incremental deviation at any given temperature.

Typical Performance Curves

*Calculating Average Temperature Coefficient (TC)



- TC in mV/°C = $\frac{\Delta V_{REF} \text{ (mV)}}{\Delta T_A}$
- TC in %/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF} \text{ at } 25^\circ\text{C}}\right) \times 100}{\Delta T_A}$
- TC in ppm/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF} \text{ at } 25^\circ\text{C}}\right) \times 10^6}{\Delta T_A}$

Test Circuits

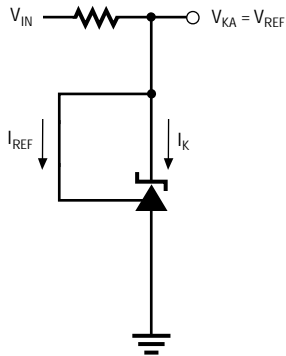


Figure 1a. Test Circuit 1

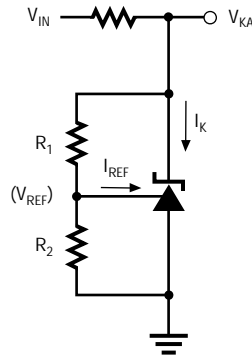


Figure 1b. Test Circuit 2

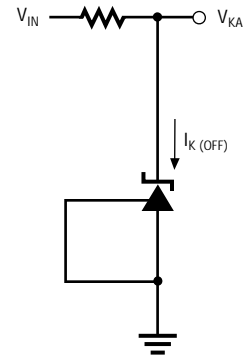
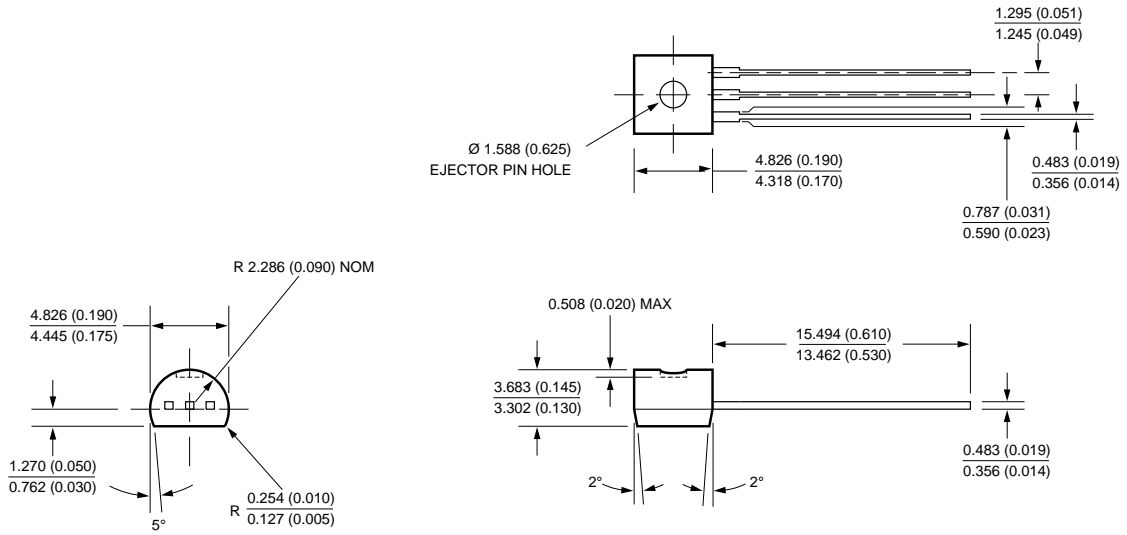


Figure 1c. Test Circuit 3

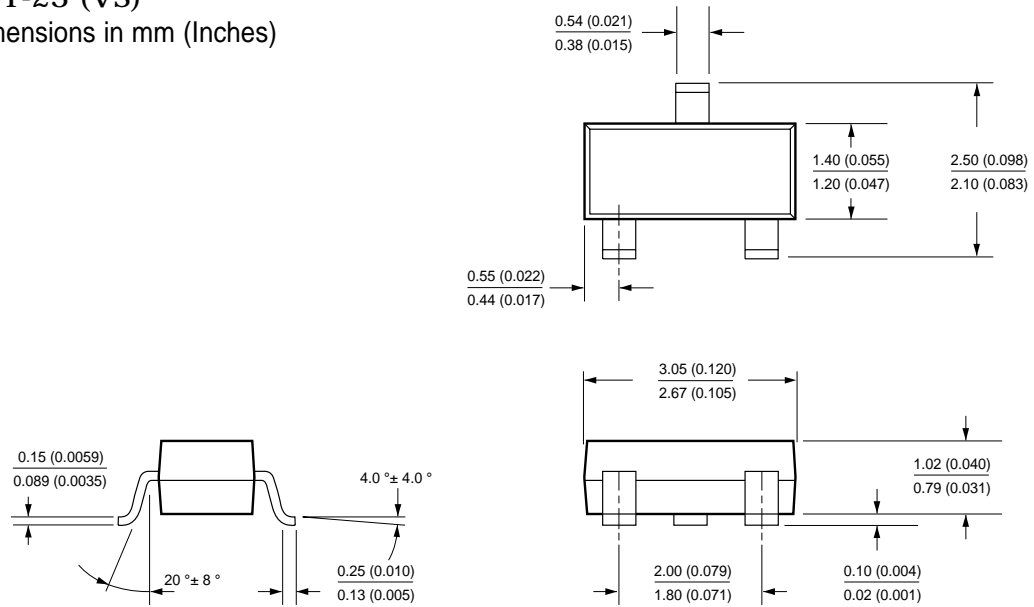
TO-92 PLASTIC (LP)

Dimensions in mm (Inches)



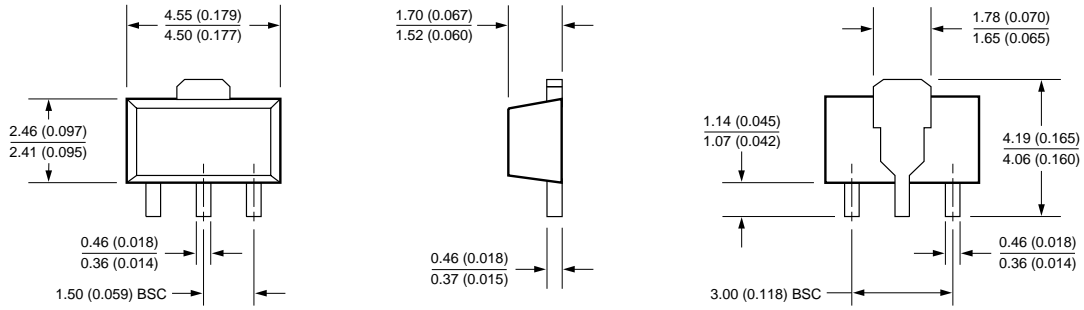
SOT-23 (VS)

Dimensions in mm (Inches)



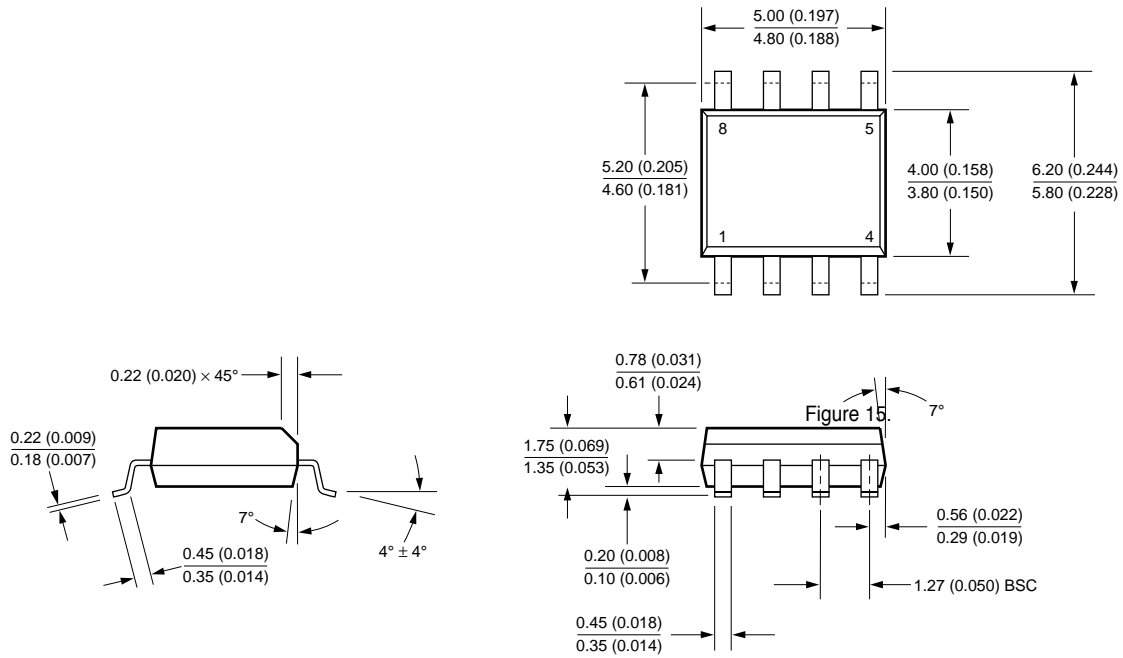
SOT-89 (S)

Dimensions in mm (Inches)



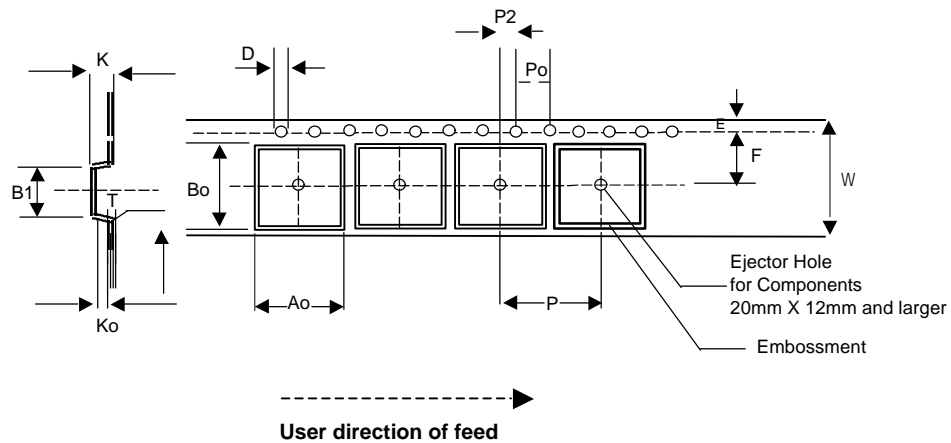
8-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)



Package Mechanical Drawing

Surface Mountable Tape & Reel Specifications in mm (inch)
 (SOIC, SOT-89, SOT-23)

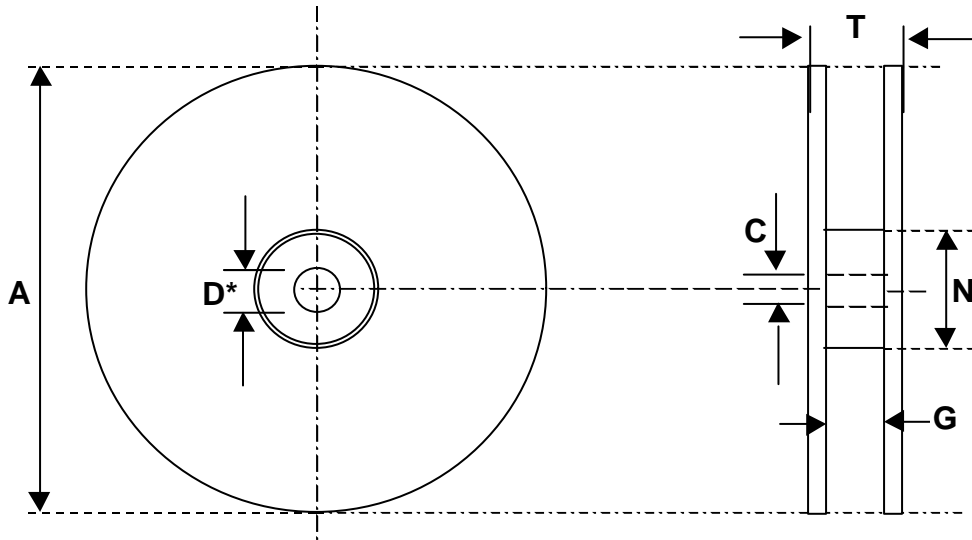


Tape Size (W)	D	E	P0	T (Max)	A0, B0, K0	T1 (Max)	Constant Dimensions
8, 12, 16, 24mm	1.55±0.05 (.061±.002)	1.75±0.10 (.069±.004)	4.0±0.10 (.157±.004)	0.400 (.016)	See Note	0.100 (.004)	

Tape Size (W)	B1 Max.	D1 Min.	F	K Max.	P2	
8 mm	4.2 (.165)	1.0 (.039)	3.5±0.05 (.138±.002)	2.4 (.094)	2.0±.05	
12 mm	8.2 (.323)	1.5 (.059)	5.5±0.05 (.217±.002)	4.5 (.177)	.079±.002	Variable Dimensions

Per Package Requirement						
Components		Tape Width (W) mm	Cavity Pitch (P) mm	Devices per Reel		
				7" Reel	13" Reel	14" Reel
SOIC	8L	12	8	-	2500	-
SOT-23	3L	8	4	3000	-	-
	5L	8	4	3000	-	-
SOT-89	4L	12	8	-	2500	-

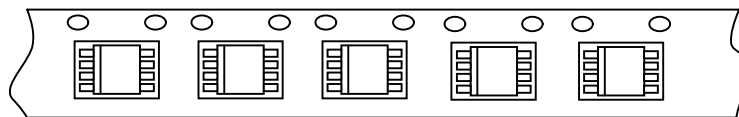
Note: Ao Bo Ko are determined by component size. The clearance between the component and the cavity must be within 0.05 [.002] min. to 0.50 [.020] max. for 8mm tape, 0.05 [.002] min to 0.65 [.026] max for 12mm tape.



REEL DIMENSIONS							
Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
8mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	8.4±1.5 0.0 (.331±.059) 0.0	14.4 (.567)
12mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	12.4±2.0 0.0 (.488±.078) 0.0	14.4 (.567)

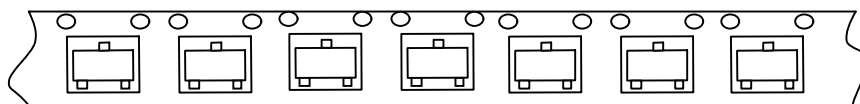
MECHANICAL POLARIZATION

SOIC DEVICES



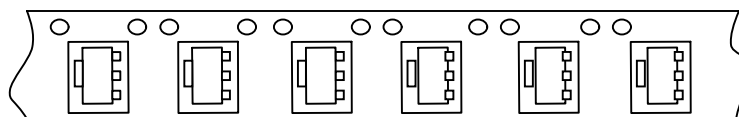
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SOT 23 3L DEVICE



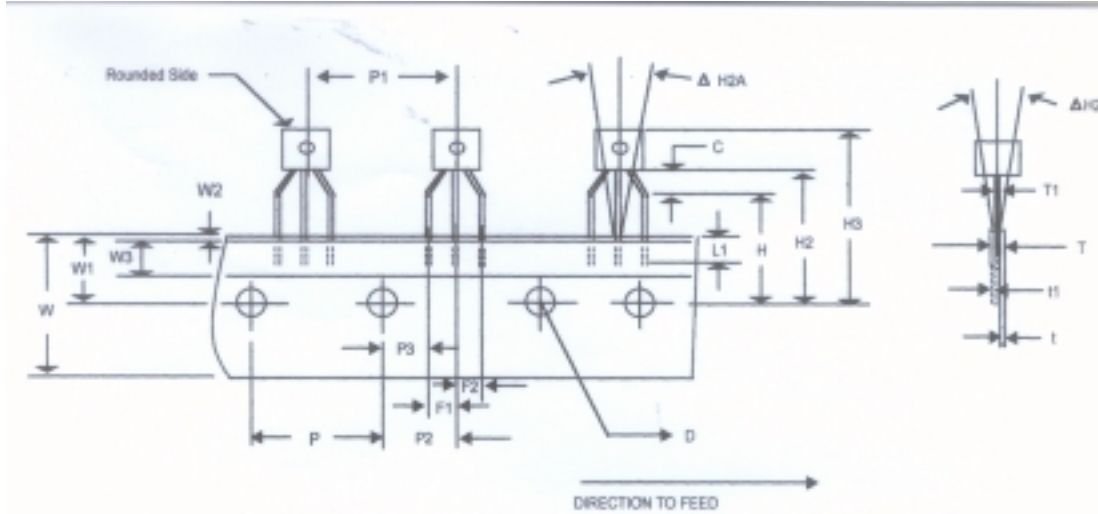
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SOT 89 DEVICE



User direction of feed →

TO-92 Tape & Reel & Ammo Pack Specifications



SYM	DESCRIPTION	NOMINAL		TOLERANCES			
		VALUE		min		max	
BOL		mm	inch	mm	inch	mm	inch
D	Feed Hole Diameter	4.0	0.157	3.8	0.150	4.2	0.165
T1 (POD)	Component Lead Thickness	0.405	0.016	0.36	0.014	0.45	0.018
F1/F2	Lead Pitch (Left / Right)	2.54	0.100	2.4	0.094	2.8	0.110
C	Bottom of Component to Seating Plane	2.50	0.098	1.50	0.059	4.00	0.157
W1	Edge to Sprocket Hole Center	9.0	0.354	8.50	0.335	9.50	0.374
H2A	Deflection (Left or Right)	0.50	0.020	0	0	0.50	0.020
H2B	Deflection (Front or Rear)	1.0	0.039	0	0	1.0	0.039
H2 (H +C)	Feed Hole to Bottom of Component	18.5	0.728	17.00	0.669	20.50	0.087
H	Height of Seating Plane	16	0.630	15.5	0.610	16.5	0.650
H3	Feed Hole Center to Overall Transistor Height	27.75	1.092	23.5	0.925	32.0	1.260
L	Defective Unit Clipped Dimension	-	-	-	-	11.0	0.433
L1	Leadwire Enclosure	2.50	0.098	2.50	0.098	-	-
P	Feed Hole Pitch	12.7	0.500	12.40	0.488	13.0	0.512
P2	Center of Feed Hole to Center Lead	6.35	0.250	6.0	0.234	6.75	0.266
P3 (P2-F1)	First Lead Spacing Dimension	3.75	0.148	3.6	0.142	3.95	0.156
P1	Center Lead to Center Lead	12.7	0.500	12.2	0.500	13.2	0.520
t1	Adhesive Tape Thickness	0.18	0.007	0.16	0.006	0.20	0.008
T (t+t1+T1)	Overall Taped Package Thickness	-	-	-	-	1.55	0.061
t	Carrier Strip Thickness	0.37	0.015	0.27	0.011	0.47	0.018
W	Carrier Strip Width (18mm)	18.00	0.709	17.5	0.689	19.0	0.748
W3	Adhesive Tape Width (6mm)	6.00	0.236	5.5	0.217	6.3	0.248
W2	Adhesive Tape Position	0.25	0.010	0	0	0.50	0.020