

**DESCRIPTION**

The AS431 is a three-terminal adjustable shunt regulator providing a highly accurate bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

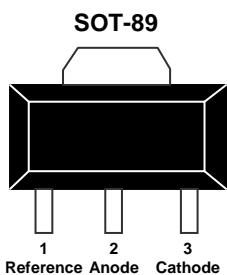
In the standard shunt configuration, the combination of low temperature coefficient (TC), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference a perfect zener diode replacement.

The AS431 precision adjustable shunt reference is offered in four bandgap tolerances:  $\pm 0.25\%$ ,  $\pm 0.5\%$ ,  $\pm 1.0\%$  and  $\pm 2.0\%$ .

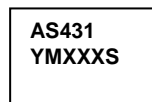
**FEATURES**

- Temperature-compensated: 30 ppm/°C
- Trimmed bandgap reference
- Internal amplifier with 150 mA capability
- Multiple temperature ranges
- Low frequency dynamic output impedance: < 150 mΩ
- Low output noise
- Robust ESD protection
- Available in Lead Free (RoHS Compliant) version.

**PIN CONFIGURATION – Top View**

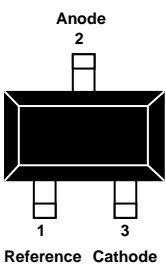


**PACKAGE TOP MARKING:**  
(For SOT-89)

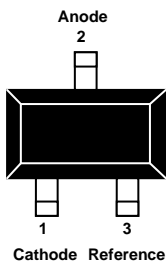


Line 1: Device  
Line 2: Lot No. Code  
YMXXX – 5 Character Lot No.  
mark excluding 1<sup>st</sup> letter  
character of lot no.  
S – Split Code

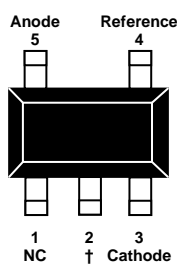
**3L SOT-23/  
VS**



**3L SOT-23/  
VF**



**5L SOT-23**



**PACKAGE TOP MARKING:**  
(For 3L/5L SOT-23)

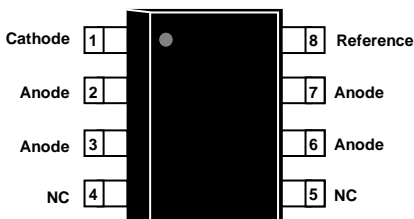


Line 1: # BBB  
# – Device Number  
(single letter code)  
BBB – Sequential Number

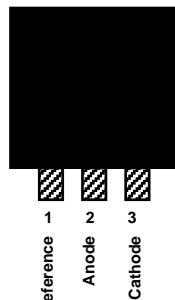
**Note:**

1. # is based on Silicon Link Device Marking Guidelines (refer to SLI form no. FM-40217)
2. BBB is based on Silicon Link Logbook Code

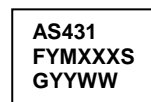
**8L SOIC**



**TO-92**



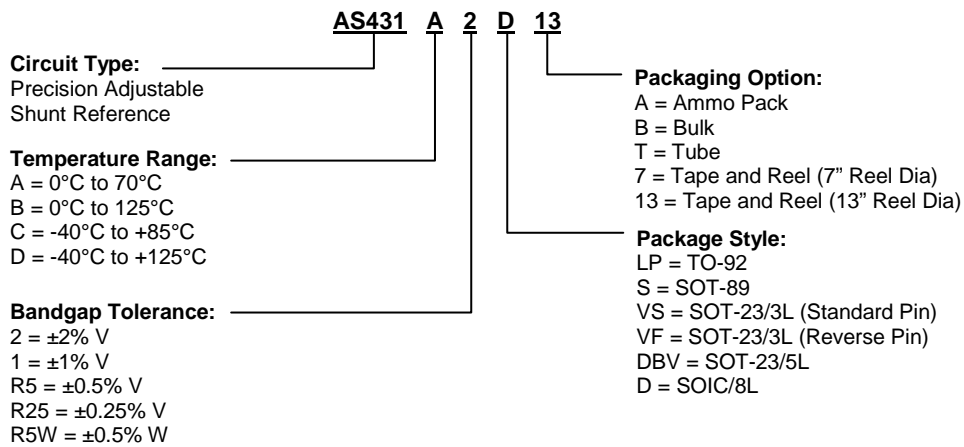
**PACKAGE TOP MARKING:**  
(For both TO-92 & 8L SOIC)



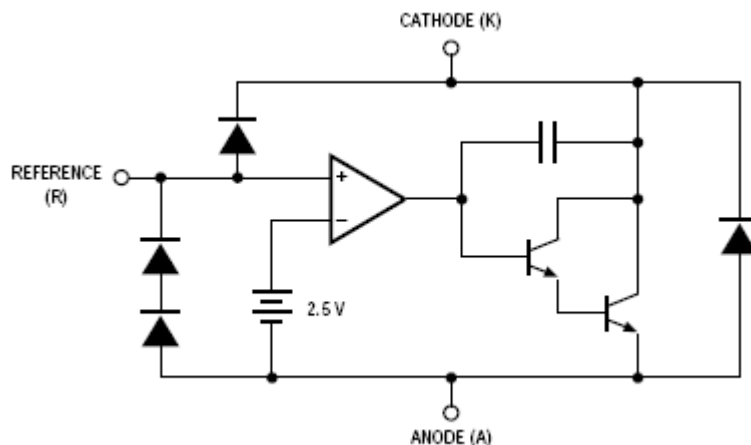
Line 1: Device  
Line 2: Lot No. Code  
F – Foundry Code (S)  
YMXXX – 5 Character Lot No.  
S – Split Code  
Line 3: Date Code  
G – Assembly Vendor Code  
YY – Year  
WW – Workweek

Note: Top marking for 1.0% 431 is A431 (applies to SOT-89, TO-92 and SOIC packages).  
Refer to Silicon Link Device Marking Guidelines.

**ORDERING INFORMATION**



**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

| Parameter                              | Symbol    | Rating     | Units |
|--|-----------|------------|-------|
| Cathode-Anode Reverse Breakdown        | $V_{KA}$  | 37         | V     |
| Anode-Cathode Forward Current          | $I_{AK}$  | 1          | A     |
| Operating Cathode Current              | $I_{KA}$  | 150        | mA    |
| Reference Input Current                | $I_{REF}$ | 10         | mA    |
| Continuous Power Dissipation at 25°C   | $P_D$     |            |       |
| TO-92                                  |           | 775        | mW    |
| 8L SOIC                                |           | 750        | mW    |
| SOT-89                                 |           | 1000       | mW    |
| SOT-23/3L                              |           | 200        | mW    |
| SOT-23/5L                              |           | 200        | mW    |
| Junction Temperature                   | $T_J$     | 150        | °C    |
| Storage Temperature                    | $T_{STG}$ | -65 to 150 | °C    |
| Lead Temperature, Soldering 10 Seconds | $T_L$     | 300        | °C    |

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



RECOMMENDED CONDITIONS

| Parameter       | Symbol   | Rating          | Unit |
|-----------------|----------|-----------------|------|
| Cathode Voltage | $V_{KA}$ | $V_{REF}$ to 20 | V    |
| Cathode Current | $I_K$    | 10              | mA   |

TYPICAL THERMAL RESISTANCES

| Package   | $\theta_{JA}$ | $\theta_{JC}$ | Typical Derating |
|-----------|---------------|---------------|------------------|
| TO-92     | 160°C/W       | 80°C/W        | 6.3 mW/°C        |
| SOIC      | 175°C/W       | 45°C/W        | 5.7 mW/°C        |
| SOT-89    | 110°C/W       | 8°C/W         | 9.1 mW/°C        |
| SOT-23/3L | 575°C/W       | 150°C/W       | 1.7 mW/°C        |
| SOT-23/5L | 575°C/W       | 150°C/W       | 1.7 mW/°C        |

ELECTRICAL CHARACTERISTICS

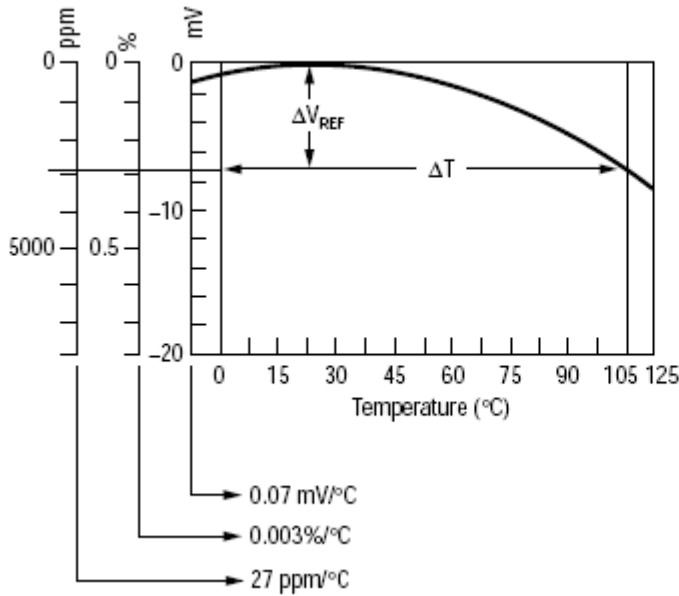
Electrical Characteristics are guaranteed over full junction temperature range (0 to 125°C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are:  $V_{KA} = V_{REF}$  and  $I_K = 10$  mA unless otherwise noted.

| Parameter                                       | Symbol                              | Test Condition                                   | AS431 (0.25%) |       |       | AS431 (0.5%) |       |       | UNIT          | TEST CIRCUIT |
|---|-------------------------------------|--|---------------|-------|-------|--------------|-------|-------|---------------|--------------|
|   |                                     |  | MIN           | TYP   | MAX   | MIN          | TYP   | MAX   |               |              |
| Reference Voltage                               | $V_{REF}$                           | $T_A = 25^\circ\text{C}$                         | 2.496         | 2.503 | 2.509 | 2.490        | 2.503 | 2.515 | V             | 1            |
|   |                                     | Over Temp.                                       | 2.475         |       | 2.530 | 2.496        |       | 2.536 | V             | 1            |
| $\Delta V_{REF}$ with Temp*                     | TC                                  |  |               | 0.07  | 0.20  |              | 0.07  | 0.20  | mV/°C         | 1            |
| Ratio of Change in $V_{REF}$ to Cathode Voltage | $\frac{\Delta V_{REF}}{\Delta V_K}$ | $V_{REF}$ to 10V                                 |               | -1.0  | -2.7  |              | -1.0  | -2.7  | mV/V          | 2            |
|   |                                     | 36V to 10V                                       |               | -0.4  | -2.0  |              | -0.4  | -2.0  |               |              |
| Reference Input Current                         | $I_{REF}$                           |  |               | 0.7   | 4     |              | 0.7   | 4     | $\mu\text{A}$ | 2            |
| $I_{REF}$ Temp Deviation                        | $\Delta I_{REF}$                    | Over Temp.                                       |               | 0.4   | 1.2   |              | 0.4   | 1.2   | $\mu\text{A}$ | 2            |
| Min $I_K$ for Regulation                        | $I_{K(\text{min})}$                 |  |               | 0.4   | 1     |              | 0.4   | 1     | mA            | 1            |
| Off State Leakage                               | $I_{K(\text{off})}$                 | $V_{REF} = 0\text{V}$ ,<br>$V_{KA} = 36\text{V}$ |               | 0.04  | 250   |              | 0.04  | 250   | nA            | 3            |
| Dynamic Output Impedance                        | $Z_{KA}$                            | $F \leq 1$ kHz<br>$I_K = 1$ to 150mA             |               | 0.15  | 0.5   |              | 0.15  | 0.5   | $\Omega$      | 1            |

| Parameter                                       | Symbol                              | Test Condition                                   | AS431 (1.0%) / (2.0%) |              |              | AS431 (0.5%) W |       |       | UNIT          | TEST CIRCUIT |
|---|-------------------------------------|--|-----------------------|--------------|--------------|----------------|-------|-------|---------------|--------------|
|   |                                     |  | MIN                   | TYP          | MAX          | MIN            | TYP   | MAX   |               |              |
| Reference Voltage                               | $V_{REF}$                           | $T_A = 25^\circ\text{C}$                         | 2.470                 | 2.495        | 2.520        | 2.510          | 2.522 | 2.535 | V             | 1            |
|   |                                     |  | <b>2.440</b>          | <b>2.490</b> | <b>2.550</b> |                |       |       |               |              |
|   |                                     | Over Temp.                                       | 2.449                 |              | 2.541        | 2.488          |       | 2.556 | V             | 1            |
|   |                                     |  | <b>2.430</b>          |              | <b>2.569</b> |                |       |       |               |              |
| $\Delta V_{REF}$ with Temp*                     | TC                                  |  |                       | 0.07         | 0.20         |                | 0.07  | 0.20  | mV/°C         | 1            |
| Ratio of Change in $V_{REF}$ to Cathode Voltage | $\frac{\Delta V_{REF}}{\Delta V_K}$ | $V_{REF}$ to 10V                                 |                       | -1.0         | -2.7         |                | -1.0  | -2.7  | mV/V          | 2            |
|   |                                     | 10V to 36V                                       |                       | -0.4         | -2.0         |                | -0.4  | -2.0  |               |              |
| Reference Input Current                         | $I_{REF}$                           |  |                       | 0.7          | 4            |                | 0.7   | 4     | $\mu\text{A}$ | 2            |
| $I_{REF}$ Temp Deviation                        | $\Delta I_{REF}$                    | Over Temp.                                       |                       | 0.4          | 1.2          |                | 0.4   | 1.2   | $\mu\text{A}$ | 2            |
| Min $I_K$ for Regulation                        | $I_{K(\text{min})}$                 |  |                       | 0.4          | 1            |                | 0.4   | 1     | mA            | 1            |
| Off State Leakage                               | $I_{K(\text{off})}$                 | $V_{REF} = 0\text{V}$ ,<br>$V_{KA} = 36\text{V}$ |                       | 0.04         | 250          |                | 0.04  | 250   | nA            | 3            |
| Dynamic Output Impedance                        | $Z_{KA}$                            | $F \leq 1$ kHz<br>$I_K = 1$ to 150mA             |                       | 0.15         | 0.5          |                | 0.15  | 0.5   | $\Omega$      | 1            |

\*Calculating Average Temperature Coefficient (TC). Refer to following page.

**AVERAGE TEMPERATURE COEFFICIENT**



- TC in mV/°C =  $\frac{\Delta V_{REF} \text{ (mV)}}{\Delta T_A}$
- TC in %/°C =  $\frac{\left(\frac{\Delta V_{REF}}{V_{REF} \text{ at } 25^\circ\text{C}}\right) \times 100}{\Delta T_A}$
- TC in ppm/°C =  $\frac{\left(\frac{\Delta V_{REF}}{V_{REF} \text{ at } 25^\circ\text{C}}\right) \times 10^6}{\Delta T_A}$

**TEST CIRCUITS**

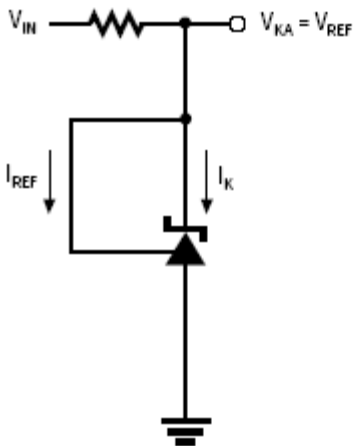


Figure 1a. Test Circuit 1

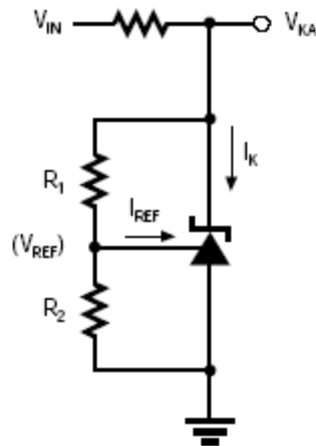


Figure 1b. Test Circuit 2

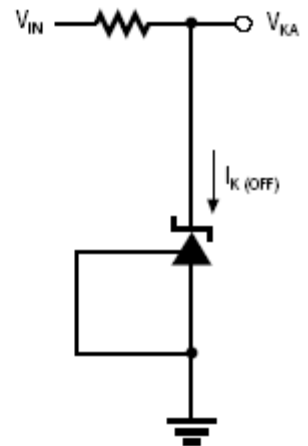


Figure 1c. Test Circuit 3



TYPICAL PERFORMANCE CURVES

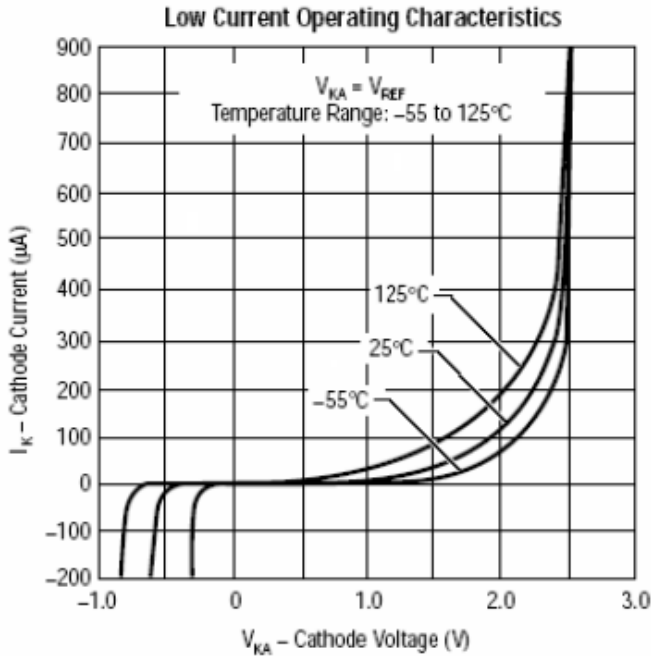


Figure 2

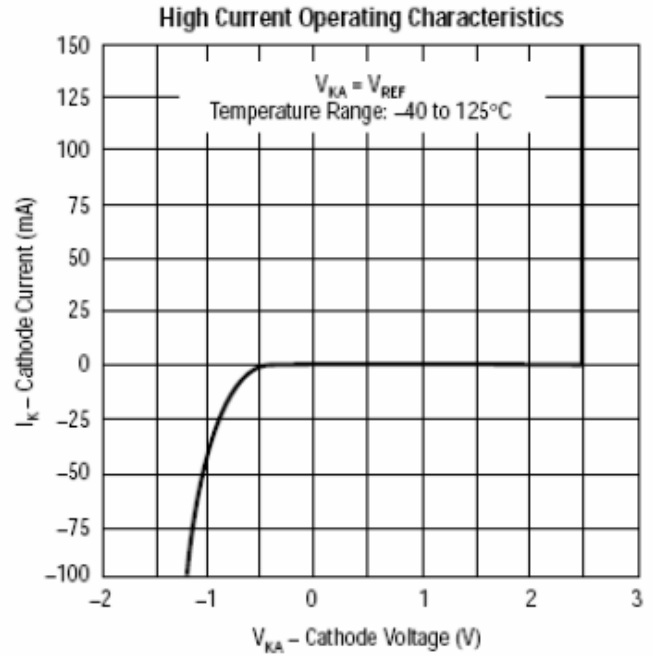


Figure 3

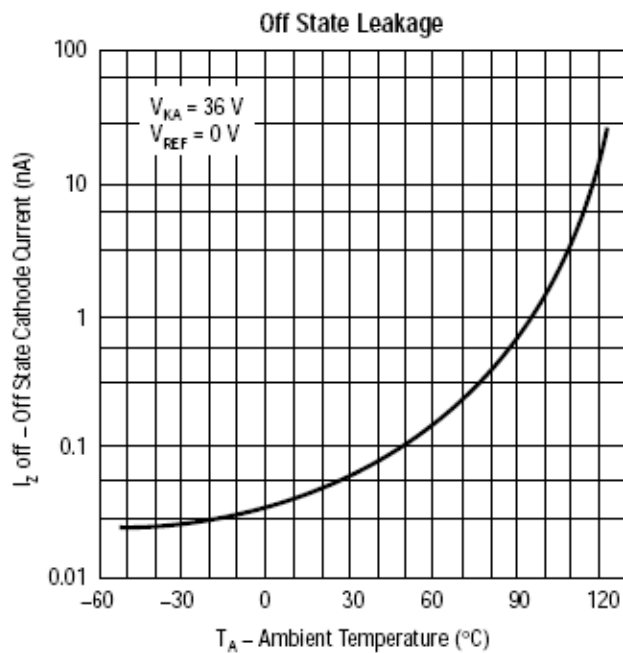


Figure 4

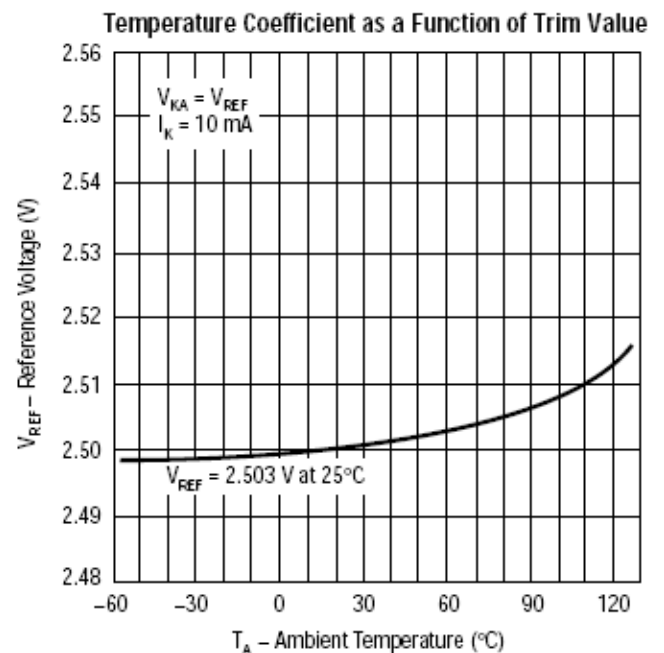


Figure 5



TYPICAL PERFORMANCE CURVES

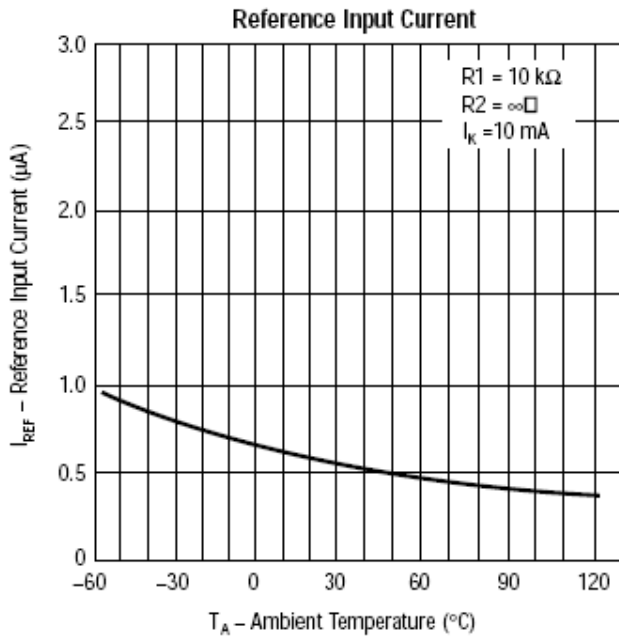


Figure 6

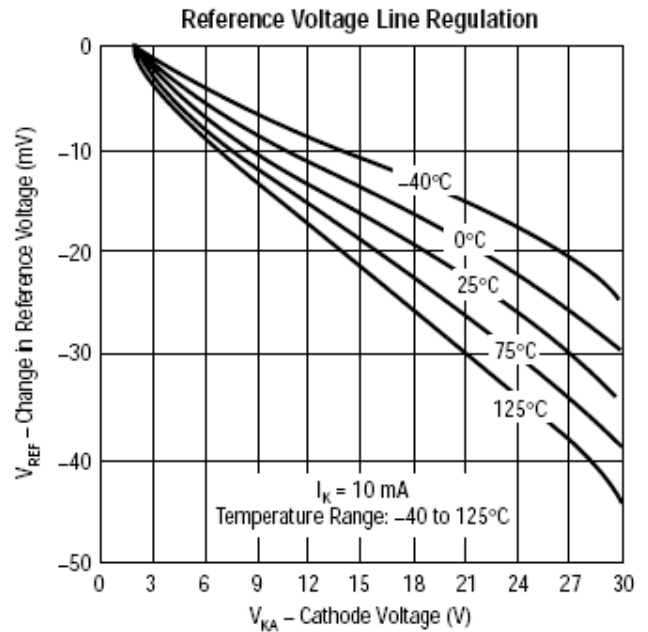


Figure 7

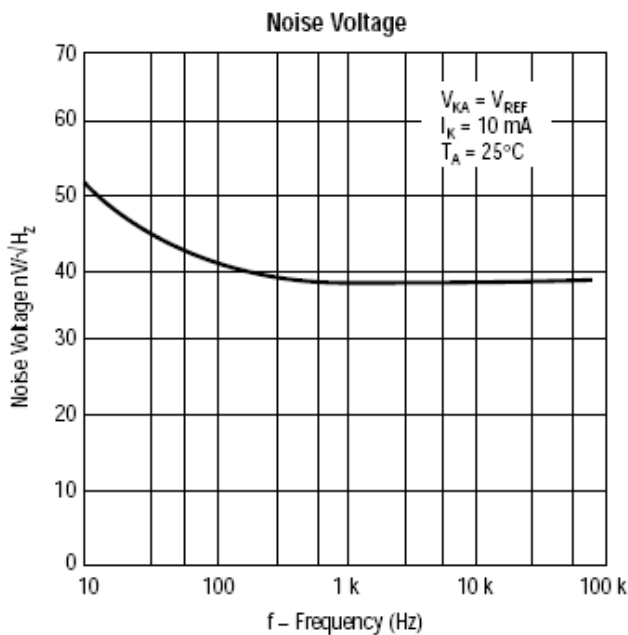


Figure 8

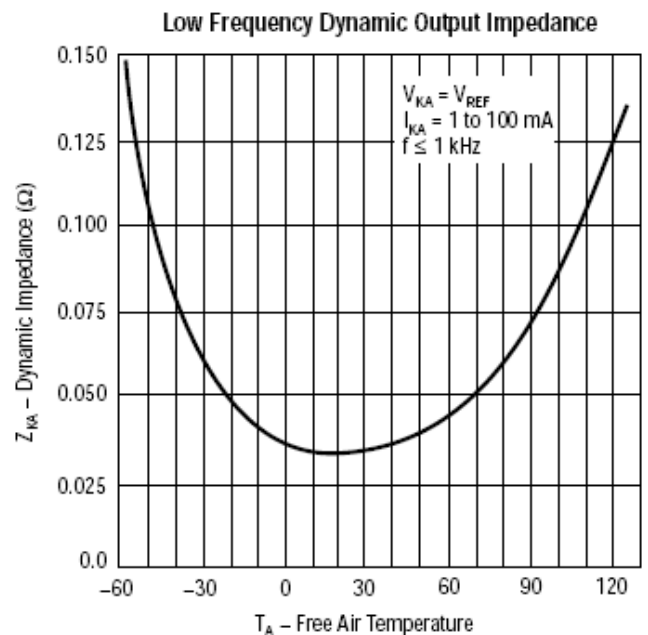


Figure 9

**TYPICAL PERFORMANCE CURVES**

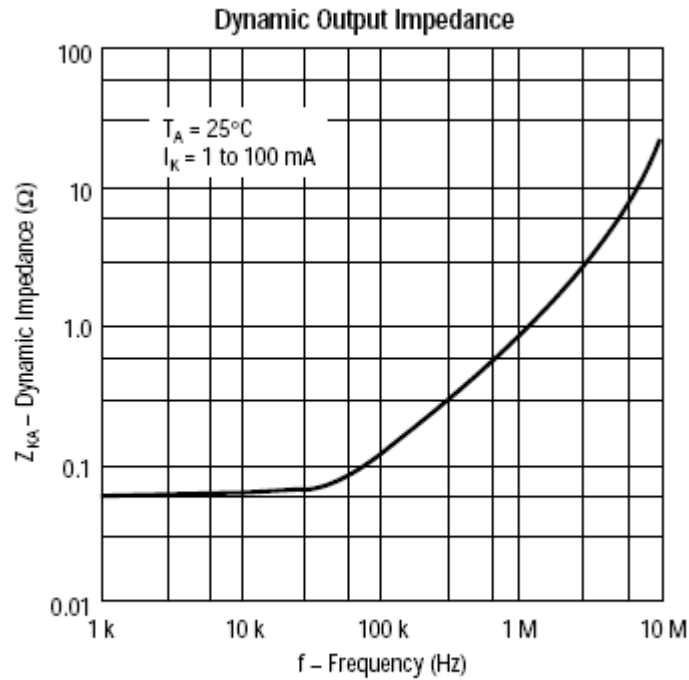


Figure 10

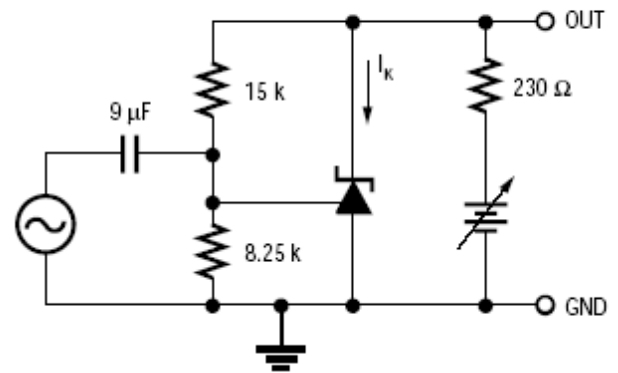
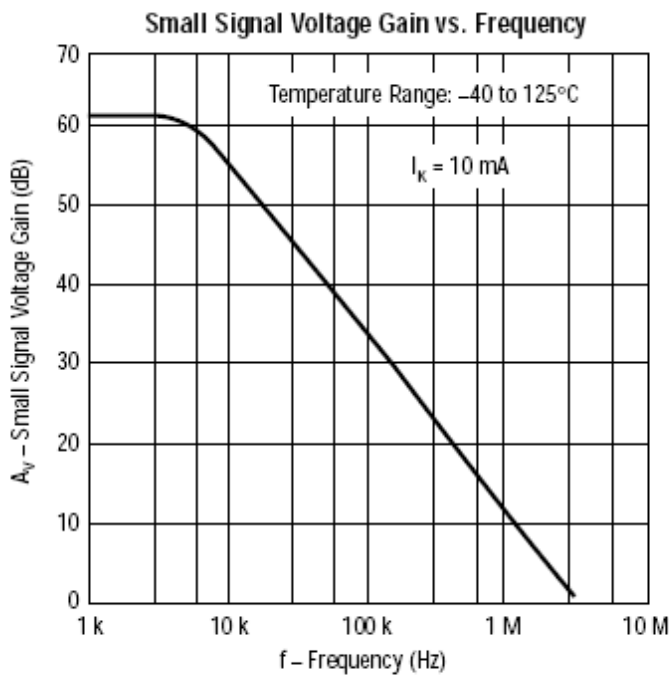


Figure 11

**TYPICAL PERFORMANCE CURVES**

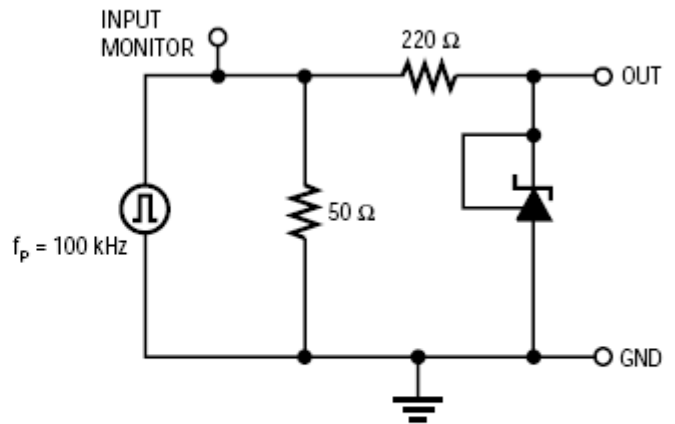
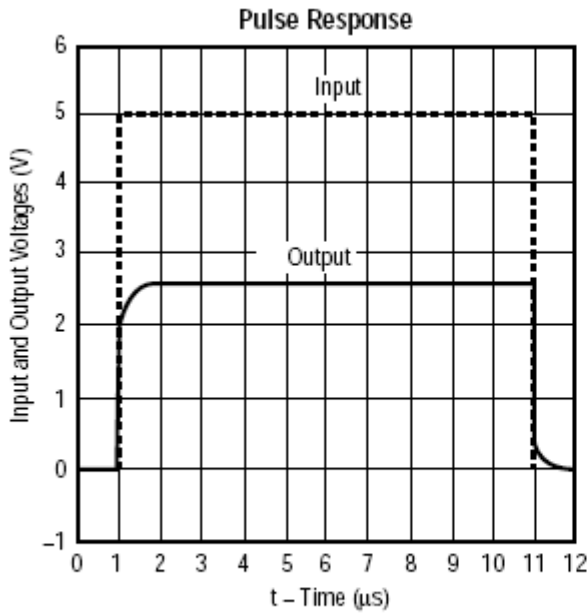


Figure 12

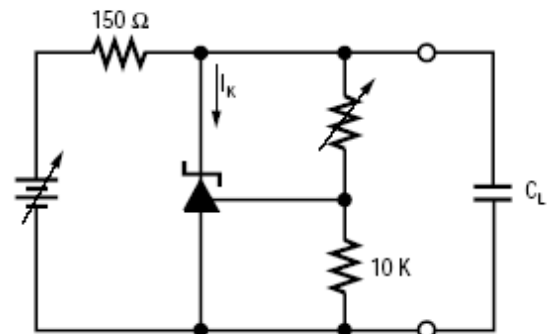
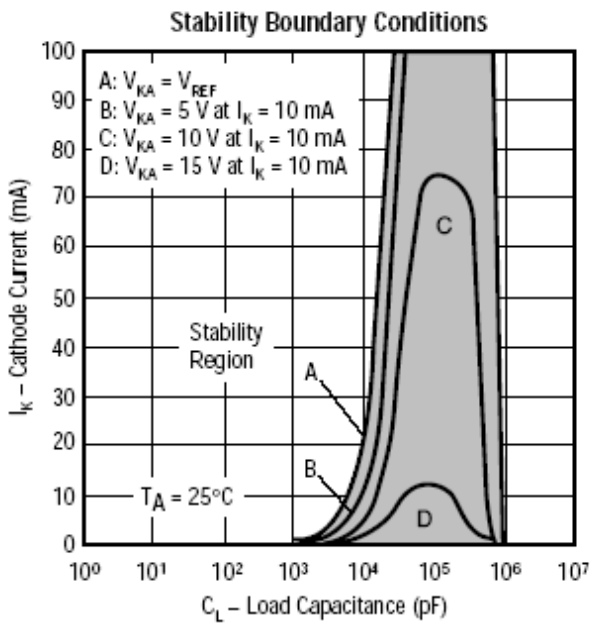


Figure 13

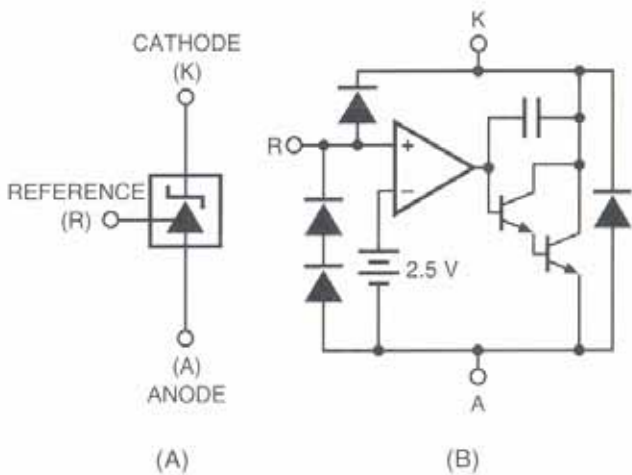
**APPLICATION INFORMATION**

The AS431 is a low-cost Precision Temperature Compensated Reference IC that is well-suited for many applications in linear and power electronics. A direct replacement for the industry standard TL431, this IC offers improved AC performance, near zero Temperature Coefficient (TC), trimmed 0.5% tolerance and is available in standard grades from 0 to 105°C and an extended temperature version, the AS1431, from -55 to 125°C.

When used with a minimum of external components, this device is ideal for a wide variety of applications including precision programmable voltage references, high speed amplifiers, comparators, linear series or shunt regulators, current sources or limiters, delay timers, voltage monitors, alarm circuits, and oscillators.

This application note demonstrates the versatility of the AS431 in typical applications and presents data useful for gaining a complete understanding of its application.

Figure 1 shows the schematic symbol and functional block diagram for the AS431. As indicated by the schematic symbol, the device can be thought of as a programmable zener diode. The functional block diagram, however, reveals a versatile IC consisting of a trimmed 2.5V precision band gap reference, a high speed amplifier (Gain BW Product = 3 MHz), ESD protection and a low impedance output stage. It is capable of shunting from 1 to 150 milliamps and has an output voltage range of 2.5 to 30 volts.



**Figure 1.** AS431 A) Schematic Symbol  
B) Functional Block Diagram

**TYPICAL APPLICATIONS**

**Precision Voltage Reference**

The most common application of the AS431 is a precision temperature compensated voltage reference as shown in Figure 2. Note that only one external resistor is required for an output voltage equal to  $V_{REF}$ . For output voltages other than  $V_{REF}$ , a simple resistor divider network is used.

**Fixed 2.5 Volt Reference**

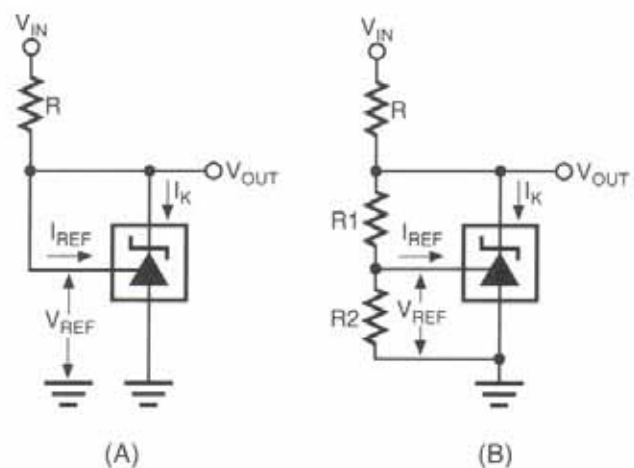
For an output voltage equal to  $V_{REF}$ , the reference input pin is connected directly to the cathode. A single resistor R is used to set the cathode current ( $I_K$ ). The value of R will depend primarily on  $V_{IN}$  and the characteristics of the load impedance that the circuit output will see (similar to selecting the series resistor for an ordinary zener diode). Generally, R should be chosen to give about 10 mA of cathode current. This will keep the power dissipation low.

Example: Determine the value of R for  $V_{IN} = 20$  volts.

The voltage across R is  $20 - 2.5 = 17.5$  V. For a desired  $I_K$  of 10mA,  $R = 17.5/0.01 = 1.75$  kΩ. Thus, an R of 1.8 kΩ will give an  $I_K$  of about 10 mA.

**Programmable Output**

To program the output of desired value between  $V_{REF}$  and 30 volts, a simple resistor voltage divider is used as shown in Figure 2B.



**Figure 2.** AS431 Precision Voltage Reference  
A) Fixed B) Programmable

$V_{OUT}$  is determined by the formula:

$$V_{OUT} = V_{REF} (1 + R1/R2) + I_{REF} \cdot R1.$$

To ensure precise regulation, low TC precision 1% resistors should be used for R1 & R2. Its values should not be so low as to cause excessive power dissipation, nor too high that an error is introduced due to changes in  $I_{REF}$  over temperature ( $I_{REF}$  is typically 0.7  $\mu A$  and deviates 0.4  $\mu A$  over the full temperature range). A good compromise is to always keep R2 at around 2 to 5 k $\Omega$  and then select R1 to obtain the desired output voltage. The circuit can be made variable by using a potentiometer for R1.

### The AS431 As An Error Amplifier

The AS431 can be used in both linear and switch mode power supplies as high gain error amplifier with a built-in temperature compensated voltage reference.

### Linear Voltage Regulator

Figure 3 shows a simple linear voltage regulator. This circuit converts an unregulated DC source (rectified AC or battery) to a low-noise, low-ripple precision-regulated DC output. The output voltage can be set to any desired value between 2.5 to 28 volts, and the output current is limited only by the series pass element.

The high gain of the AS431 allows this circuit to achieve a line/load regulation of typically 0.03% or better, depending on the application.

### Switch Mode Power Supply

The AS431 can be similarly used in switch mode power supplies as shown Figure 4. The only difference is the AS431 does not control the output voltage directly as in the linear regulator.

Instead, it provides an amplified error signal to the PWM circuitry that in turn controls the on/off ratio of the switching device(s), thereby regulating the output voltage. Also, because of the phase shifts and delays associated with the modulator and filter components in switching power supplies, a more elaborate compensation network is required in the control loop to optimize the gain/phase characteristics of system. The network type and values are chosen so as to ensure stability and proper transient response.

Note that there are many different types of switching power supply topologies having different compensation, isolation and PWM configurations. The AS431 and associated circuitry, however, are essentially the same in all cases except for component values, the type of compensation network used and location (it may be located on the primary side in some applications).

The AS431 may also be used for other functions in a switch mode power supply. For example, it can be used as a reference or a comparator in the housekeeping, input/output monitoring, temperature control, or alarm circuitry. Or, as the reference/error amplifier in a MagAmp or linear auxiliary output regulator. Figure 6 illustrates several of these applications.

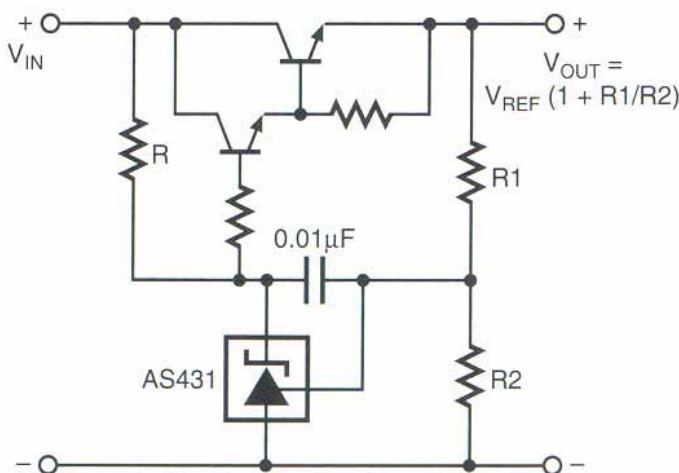
### Frequency Compensation

Frequency compensation of a power supply control loop is achieved with an external compensation network, typically connected between the reference and cathode pins of the AS431. The type of network used can be as simple as a single capacitor, or as elaborate as a dual zero-pole pair network, depending on the power supply's topology. A typical single zero-pole pair compensation network is shown in Figures 4 and 5.

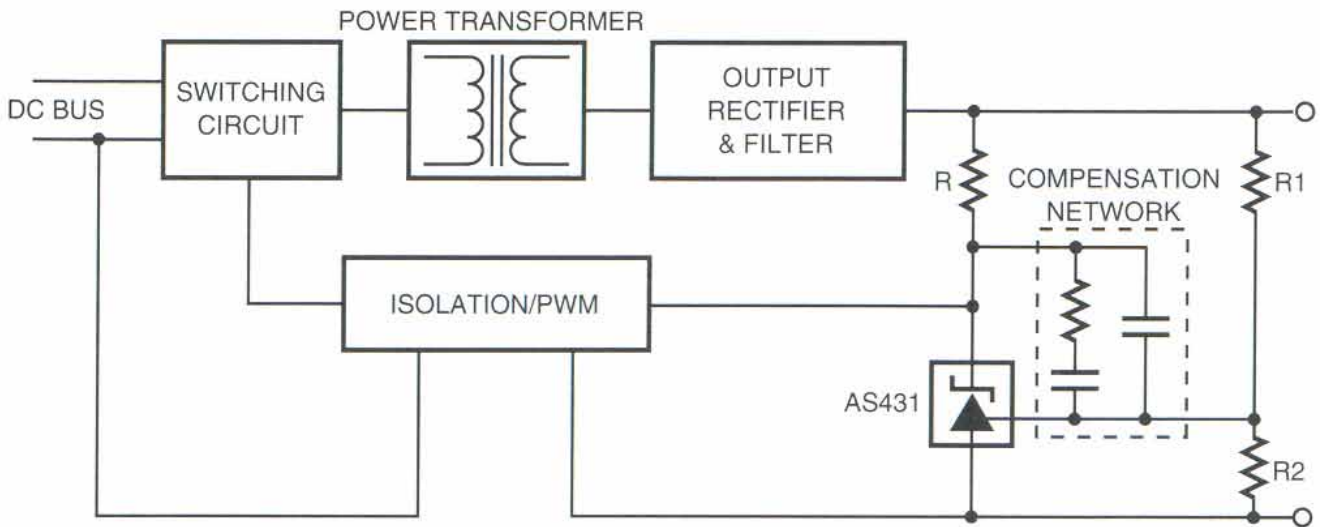
The AS431 typically has 55 dB of gain from DC to 6 kHz, where it rolls off at a 6 dB per octave rate, reaching 0 dB at 3 MHz. Further information characterizing the performance of the AS431 over frequency can be found in the AS431 Data Sheet. Due to the complexity of frequency compensation network design and the vast number of power supply topologies possible, a detailed discussion is beyond the scope of this application note. However, the information provided is useful in determining the compensation needed for a particular application.

### The AS431 as a MagAmp Controller

Post regulation is required in many cases for one or more outputs of a switch-mode power supply. Linear regulators incorporating the AS431 are adequate for most low current outputs. When high current outputs are required, a MagAmp (saturable-core) regulator is usually used because of its high efficiency.



**Figure 3.** Linear Regulator Using the AS431 as a Reference/ Error Amplifier



**Figure 4.** A Switch-Mode Power Supply Using the AS431 as a Reference/ Error Amplifier

Generally speaking, a MagAmp is a pulse-width modulated buck regulator circuit that uses a saturable core inductor as the switching element. The inductor initially has a high inductance that blocks a pre-determined number of volt-seconds. Upon saturation, the induction reverts to a very low impedance, which allows current to flow to the output with little loss. The number of volt-seconds blocked in each cycle is defined by the control circuitry and varies in accordance with changes in line and load, providing tight regulation at the output.

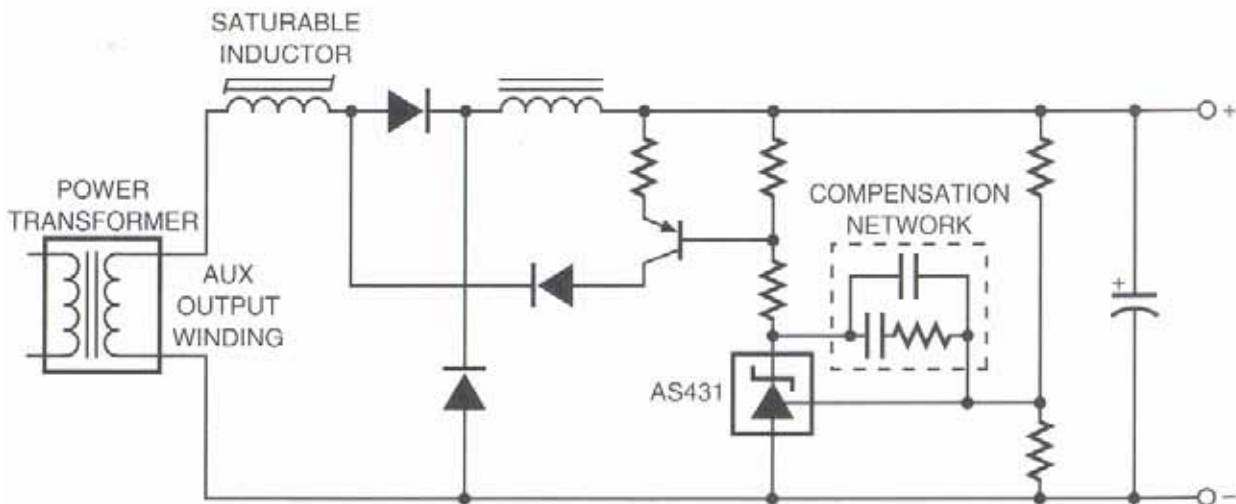
The AS431 is an ideal low-cost MagAmp controller, for it contains all the necessary control functions needed (precision reference, high gain error amplifier and an output stage) in a small package.

A schematic diagram of a typical MagAmp post regulator using the AS431 is shown in Figure 5. Since this circuit constitutes a closed loop system, frequency compensation of the error amplifier is necessary.

#### Other Applications

The AS431 also can replace an ordinary zener diode in any circuit where a higher accuracy and temperature stability is required. Viewing the AS431 as a high gain transistor with a  $V_{BE}$  of 2.5 V increases usage possibilities. Applications for this device are limited only by the imagination.

Several practical applications are illustrated in Figure 6.



**Figure 5.** An AS431 Controlled MagAmp Post Regulator

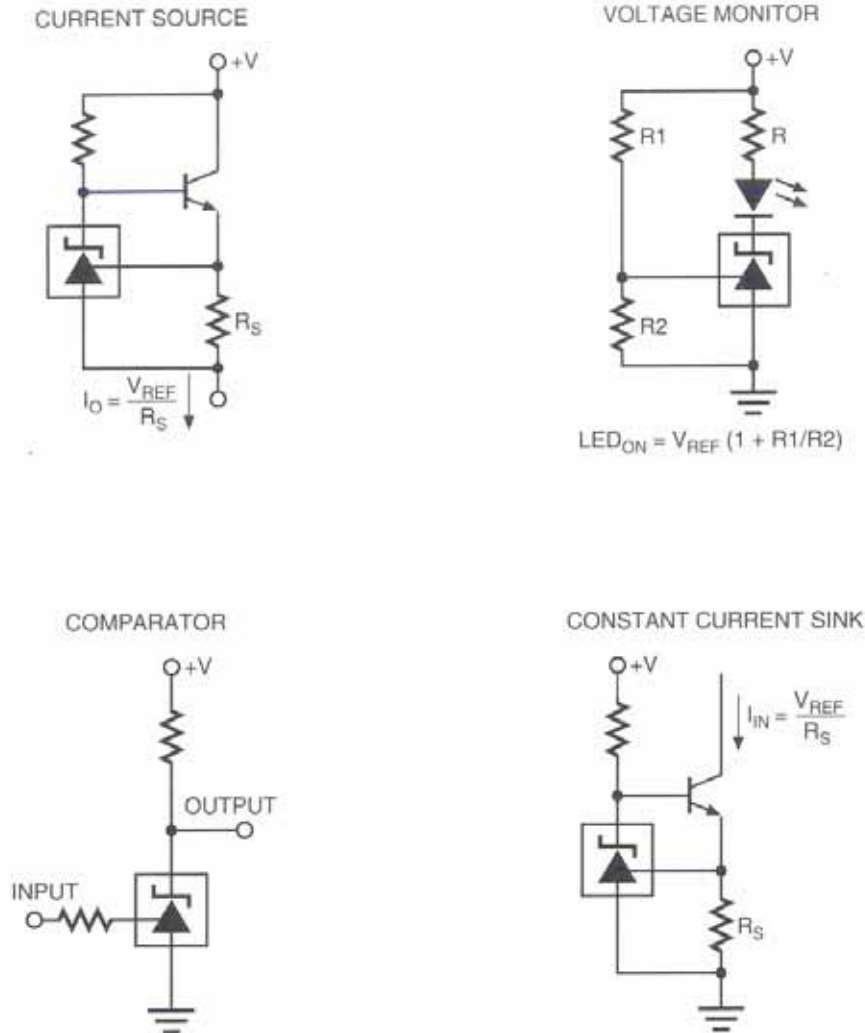


Figure 6. Typical AS431 Applications

## SECONDARY SIDE ERROR AMPLIFIER USING THE AS431

### I. Introduction

One of the most important safety regulations to which an off-line power supply must conform is input to output electrical isolation. This isolation requirement prevents the power supply control IC from directly sensing both the input line and output voltages. In the case of primary side control the output regulation information, an error voltage, must be transferred from the secondary side. This application note discusses a simple way of transmitting regulation information across the electrical isolation using an AS431 and a conventional 4N27 opto-coupler.

### II. Power Supply Circuit

Figure 1 illustrates a simple flyback regulator. The AS3842, a low-cost current mode control IC, is configured to regulate the power supply from the primary side. The AS431 acts as a reference and a feedback error amplifier to sense the output voltage and generate a corresponding error voltage. This error voltage is then converted to an error current and coupled to the primary side through a 4N27 opto-coupler.

### III. Opto-Coupler

Recently, opto-coupler manufacturers have made major improvements in opto-coupler processing and packaging technologies, resulting in tighter current transfer ratio (CTR) tolerances and better long-term reliability.

When designing the opto-coupler feedback circuitry, the designer should note the opto-coupler forward diode current. The forward diode current sets the device's CTR and effects the long-term reliability of the device. Similar to a lamp filament, the opto-coupler diode can be worn out or degraded more quickly if it is subjected

Also, the opto-coupler's unity gain bandwidth increases with forward diode current. The modulation of the gain bandwidth is caused by variations in the transconductance of the output transistor. In addition, the Miller capacitor from the base to collector of the output transistor damps out the effects of the opto-coupler's gain variance. A properly designed opto-coupler circuit not only increases long-term reliability of the regulator but also ensures a superior loop response.

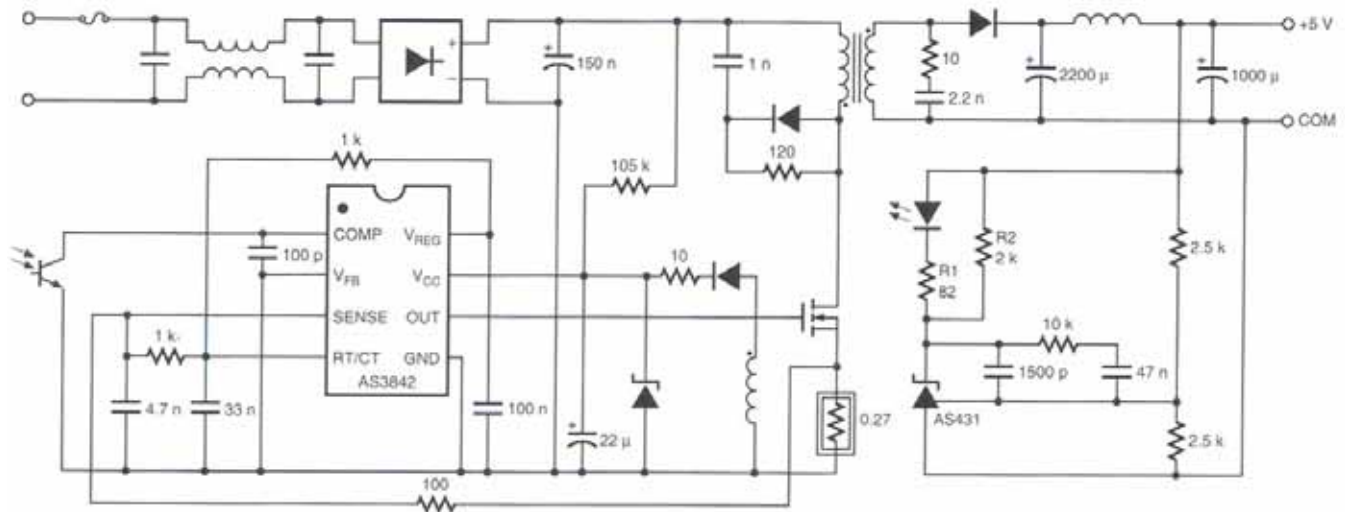


Figure 1. A 40W Flyback Power Regulator

### IV. Design Example

Figure 2 shows the amplifier feedback section of the flyback power supply. To keep the 5V output regulated, the  $V_{COMP}$  voltage must track the output voltage. The output voltage is first divided down by two  $2.5\text{ k}$  resistors, and its result is fed into an AS431 error amplifier network. The error amplifier output,  $V_{CATHODE}$ , is then converted to a proportional opto-coupler diode current. The opto-coupler bridges the isolation barrier and generates an output collector current proportional to the input diode current. Since the opto-coupler output is connected to the  $V_{COMP}$  pin, the opto-coupler output current is the  $I_{COMP}$  source current. In a normal operating condition, a higher output voltage causes  $V_{CATHODE}$  to drop and results in a high diode current and  $I_{COMP}$  source current and consequently a lower  $V_{COMP}$ . A lower  $V_{COMP}$  decreases the PWM duty cycle and therefore decreases the regulator output voltage. The result is a regulated output. A determination of the opto-coupler diode operating current and small signal loop gain follows.

#### IVa. Opto-Coupler Operating Current

This design example shows the diode operating current as determined by the maximum  $I_{COMP}$  source current. In order for  $V_{COMP}$  to decrease linearly with increasing  $I_{COMP}$  source current,  $I_{COMP}$  has to operate in a linear region slightly above the maximum  $I_{COMP}$  source current. The linear is depicted in Figure 3.

Since the  $I_{COMP}$  source current is equal to the opto-coupler output current, the opto-coupler output current also modulates in the same  $I_{COMP}$  linear region. With a known opto-coupler output current, the input diode current,  $I_{DIODE}$ , can then be obtained from the output current versus diode current curve on the opto-coupler data sheet. Figure 4 illustrates the output current versus diode current curve of the 4N27 opto-coupler.

The 4N27 data sheet guarantees a minimum of 0.1 CTR at 10 mA diode current.

The typical AS3842 maximum  $I_{COMP}$  source current is  $800\text{ }\mu\text{A}$ . Using Figure 4, and assuming 0.1 CTR at 10 mA diode current, the forward diode current required to generate  $800\text{ }\mu\text{A}$  of opto-coupler current is 8 mA.

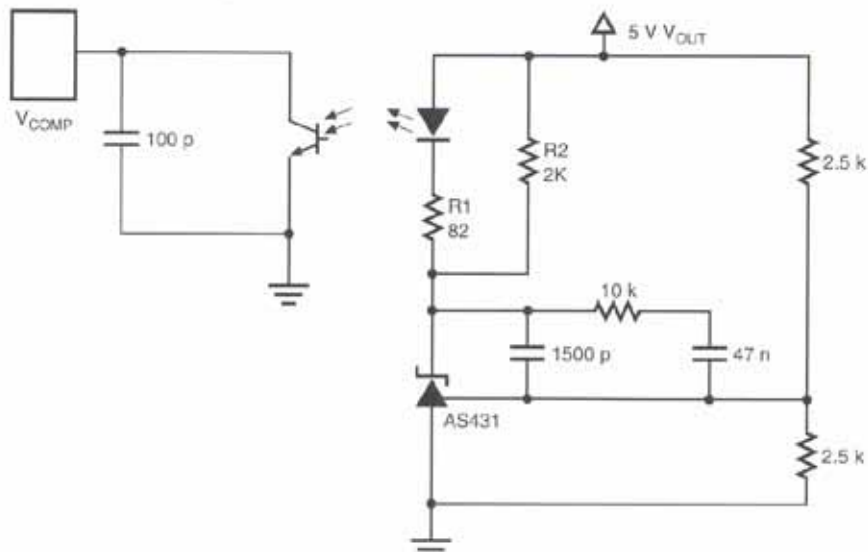


Figure 2.

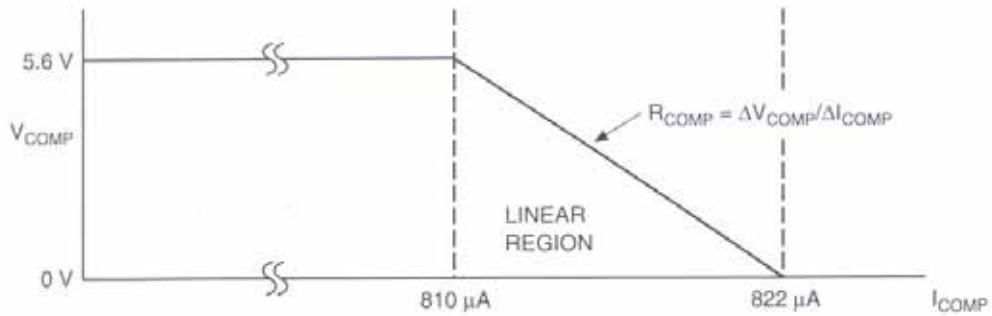
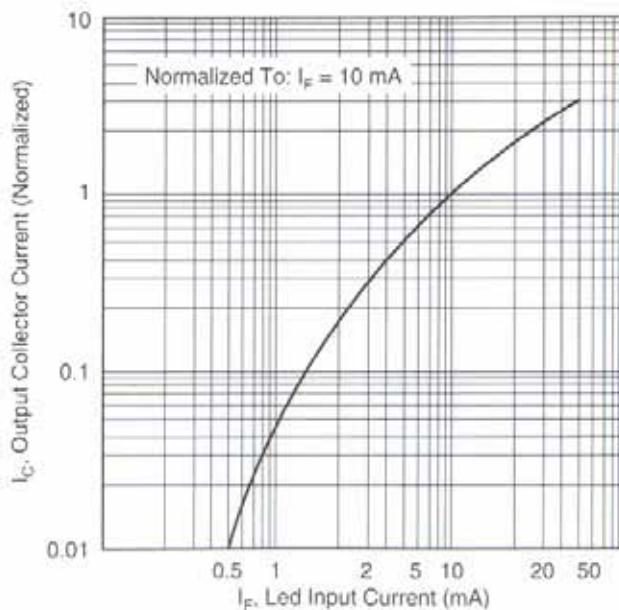


Figure 3.  $V_{COMP}$  VS  $I_{COMP}$





**IVb. AC Gain Analysis**

Once the opto-coupler diode current is determined, the current limiting resistor R1 of Figure 2 can then be chosen to guarantee good output regulations and proper dynamic loop response. The AS431 cathode voltage,  $V_{CATHODE}$  is a function of the diode operating current,  $I_{DIODE}$ , and the value of R1. Also,  $V_{CATHODE}$  must be greater than 2.5V for proper operation.

$$\begin{aligned} V_K &= V_O - V_D - (I_D \cdot R1) > 2.5V & (1) \\ &= 5.0V - 1.2V - (8 \text{ mA} \cdot R1) > 2.5V \\ &= 3.8 - (8 \text{ mA} \cdot R1) > 2.5V \\ R1 &< 162 \Omega \\ &= 82 \Omega \text{ (chosen)} \\ V_K &= 3.14 V \end{aligned}$$

R1 also plays a significant role in controlling the open loop gain of the power supply. The following equations derive the small signal AC gain from  $V_{CATHODE}$  to  $V_{COMP}$ .

$$\begin{aligned} I_{COMP} &= I_D \cdot CTR & (2) \\ &= \frac{(V_O - V_K)}{R1} \cdot CTR \end{aligned}$$

$$\begin{aligned} \frac{\Delta I_{COMP}}{\Delta V_K} &= - \frac{CTR}{R1} & (3) \end{aligned}$$

At the steady state condition,  $V_{COMP}$  is in the linear region,

$$\begin{aligned} \frac{\Delta V_{COMP}}{\Delta V_K} &= \frac{\Delta I_{COMP}}{\Delta V_K} \cdot \frac{\Delta V_{COMP}}{\Delta I_{COMP}} & (4) \\ &= \frac{CTR}{R1} \cdot R_{COMP} \end{aligned}$$

From figure 3:

$$\begin{aligned} R_{COMP} &= \frac{\Delta V_{COMP}}{\Delta I_{COMP}} \\ &= \frac{0.1}{(822 - 810) \mu A} \\ &= 509 \text{ k}\Omega \end{aligned}$$

Applying equation (4):

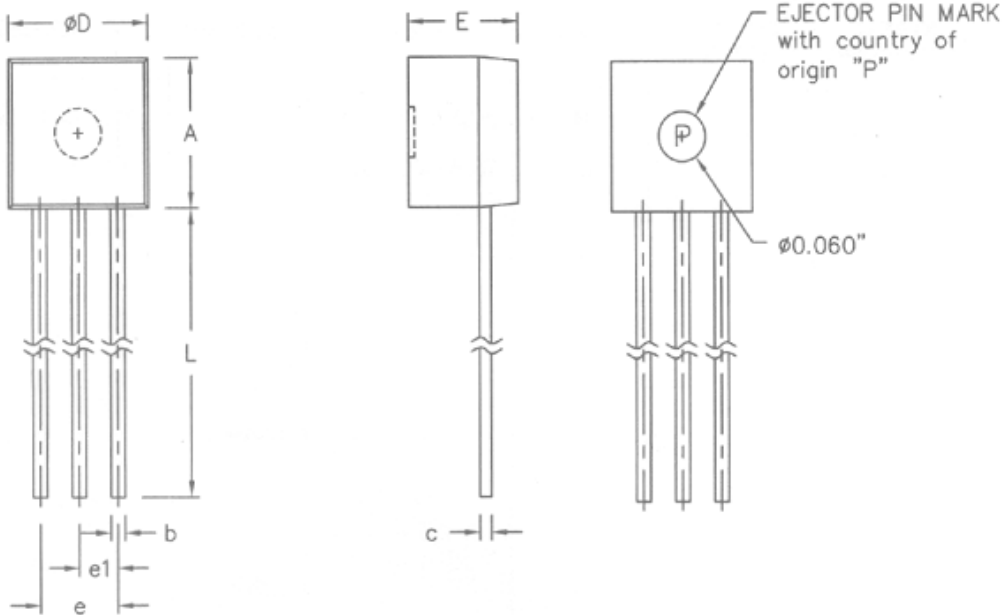
$$\begin{aligned} \frac{\Delta V_{COMP}}{\Delta V_K} &= \frac{0.1}{82 \Omega} \cdot (509 \text{ k}\Omega) \\ &= 620 \\ &= 55.9 \text{ dB} \end{aligned}$$

**IVc. Other Considerations**

R2, a 2 k $\Omega$  resistor in parallel with the opto-coupler diode and R1, provides the minimum cathode current required to keep the AS431 operating when a minimum opto-coupler diode current is required. In addition, a small filter capacitor is placed close to the  $V_{COMP}$  pin of the control IC to attenuate high frequency switching noise being picked up by the metal trace from the opto-coupler to the control IC. Since the location of the pole in the opto-coupler small signal response varies significantly with the dc operating point of the opto-coupler, a resistor can be added from the  $V_{REG}$  to  $V_{COMP}$  pin to supply additional bias current to stabilize the loop.

**TO-92 PACKAGE DIMENSION**

**3-Lead TO-92 Plastic Package**  
**SLI Package Code: LP**

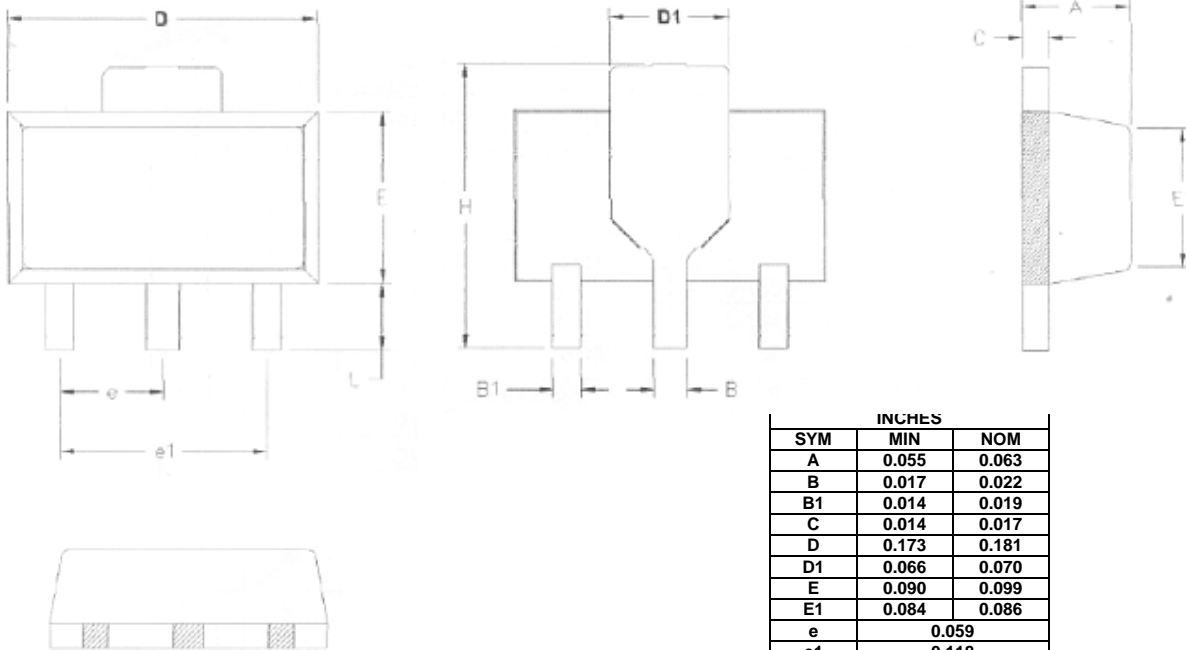


| SYMBOL   | INCHES |       |       |
|----------|--------|-------|-------|
|          | MIN    | NOM   | MAX   |
| A        | 0.176  | 0.180 | 0.184 |
| b        | 0.015  | 0.018 | 0.022 |
| c        | 0.014  | 0.015 | 0.020 |
| $\phi D$ | 0.176  | 0.180 | 0.184 |
| e        | 0.098  | 0.100 | 0.102 |
| e1       | 0.048  | 0.050 | 0.052 |
| E        | 0.136  | 0.140 | 0.144 |
| j        | 0.166  | 0.170 | 0.174 |
| L        | 0.530  | 0.550 | 0.570 |
| S1       | 0.031  | 0.035 | 0.039 |

- NOTES:**
1. ALL DIMENSIONS IN INCHES.
  2. A MECHANICAL TOLERANCE OF  $\pm 0.002''$  APPLIES TO ALL DIMENSIONS WHERE NO TOLERANCE IS EXPLICITLY GIVEN.
  3. BASED FROM JEDEC T0-226 VARIATION AA OUTLINE.

**SOT-89 PACKAGE DIMENSION**

3-Lead SOT-89 Plastic  
Surface Mounted Package  
SLI Package Code: S



| INCHES |       |       |
|--------|-------|-------|
| SYM    | MIN   | NOM   |
| A      | 0.055 | 0.063 |
| B      | 0.017 | 0.022 |
| B1     | 0.014 | 0.019 |
| C      | 0.014 | 0.017 |
| D      | 0.173 | 0.181 |
| D1     | 0.066 | 0.070 |
| E      | 0.090 | 0.099 |
| E1     | 0.084 | 0.086 |
| e      | 0.059 |       |
| e1     | 0.118 |       |
| H      | 0.155 | 0.167 |
| L      | 0.029 | 0.041 |

**NOTES:**

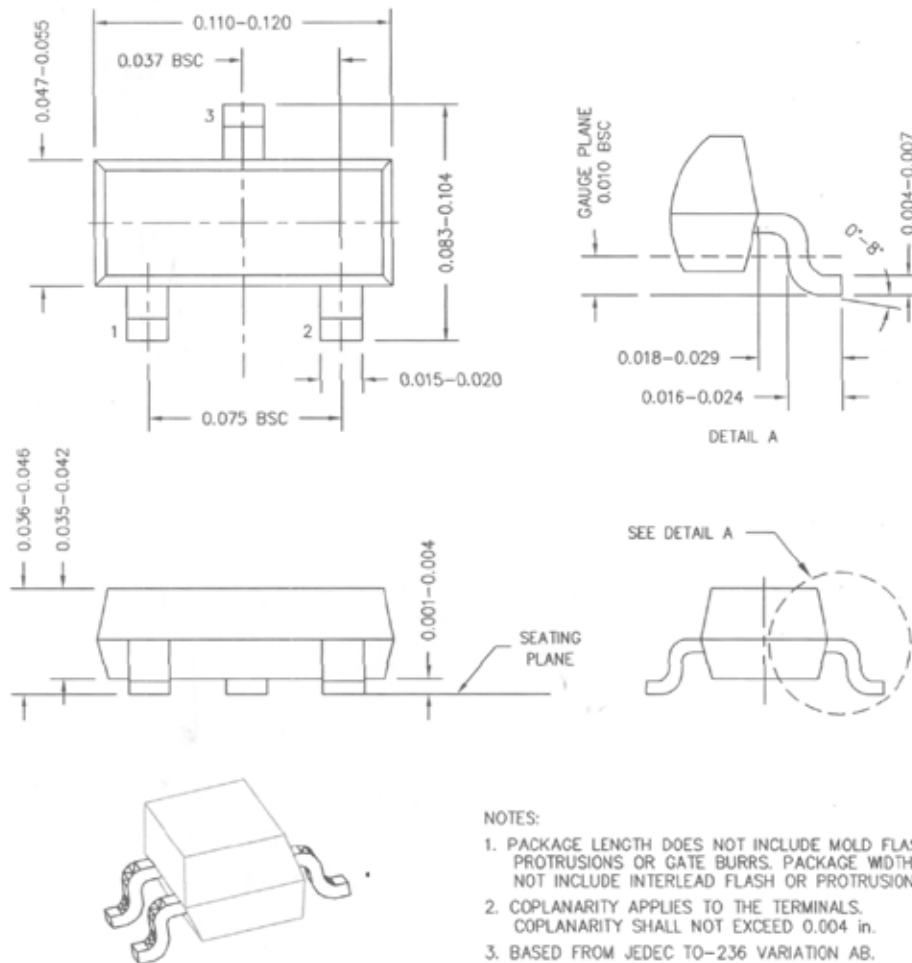
1. TOP PACKAGE ANGLE IS 9° +1°/-2° TOLERANCE. BOTTOM PACKAGE ANGLE IS 3° MAX.
2. PACKAGE CORNER RADIUS IS 5 MILS MAX ON ALL CORNERS.
3. SHINNY PACKAGE FINISH ON ALL SIDES EXCEPT TOP SIDE FINISH IS MINIMUM MATTE OF 10-14VDI.

NOTE: ALL DIMENSION ARE IN INCHES



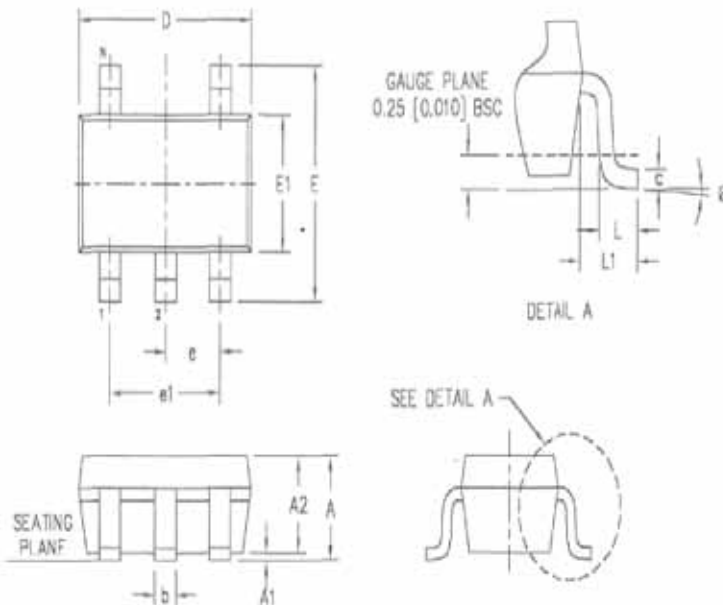
3L-SOT23 PACKAGE DIMENSION

3-Lead SOT-23 Plastic  
Surface Mounted Package  
SLI Package Code: VS



**5L-SOT23 PACKAGE DIMENSION**

**5-Lead SOT23 Plastic  
Surface Mounted Package  
SLI Package Code: DBV**

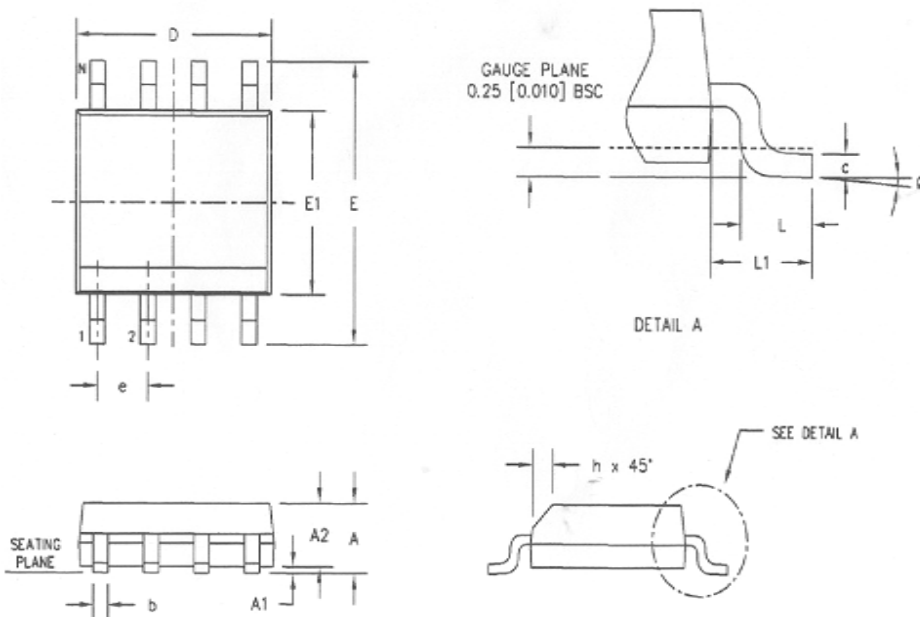


| SYM | DIMENSION IN INCHES |       |       | DIMENSION IN MM |      |      |
|-----|---------------------|-------|-------|-----------------|------|------|
|     | MIN                 | NOM   | MAX   | MIN             | NOM  | MAX  |
| A   | 0.045               | 0.049 | 0.053 | 1.14            | 1.24 | 1.35 |
| A1  | 0.002               | 0.004 | 0.006 | 0.05            | 0.10 | 0.15 |
| A2  | 0.043               | 0.045 | 0.047 | 1.09            | 1.14 | 1.19 |
| b   | 0.012               | 0.014 | 0.016 | 0.30            | 0.35 | 0.40 |
| c   | 0.003               | 0.006 | 0.009 | 0.08            | 0.15 | 0.22 |
| D   | 0.113               | 0.115 | 0.117 | 2.87            | 2.92 | 2.97 |
| E1  | 0.061               | 0.064 | 0.066 | 1.55            | 1.63 | 1.68 |
| E   | 0.105               | 0.110 | 0.115 | 2.67            | 2.79 | 2.92 |
| e   | 0.037               |       |       | 0.95            |      |      |
| e1  | 0.075               |       |       | 1.90            |      |      |
| L   | 0.014               | 0.016 | 0.018 | 0.35            | 0.40 | 0.45 |
| L1  | 0.021               | 0.023 | 0.025 | 0.53            | 0.58 | 0.64 |
| Ø   | 0*                  | -     | 8*    | 0*              | -    | 8*   |

**NOTE:**  
1. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.

**8L-SOIC PACKAGE DIMENSION**

**8-Lead SOIC Plastic  
Surface Mounted Package  
SLI Package Code: D**

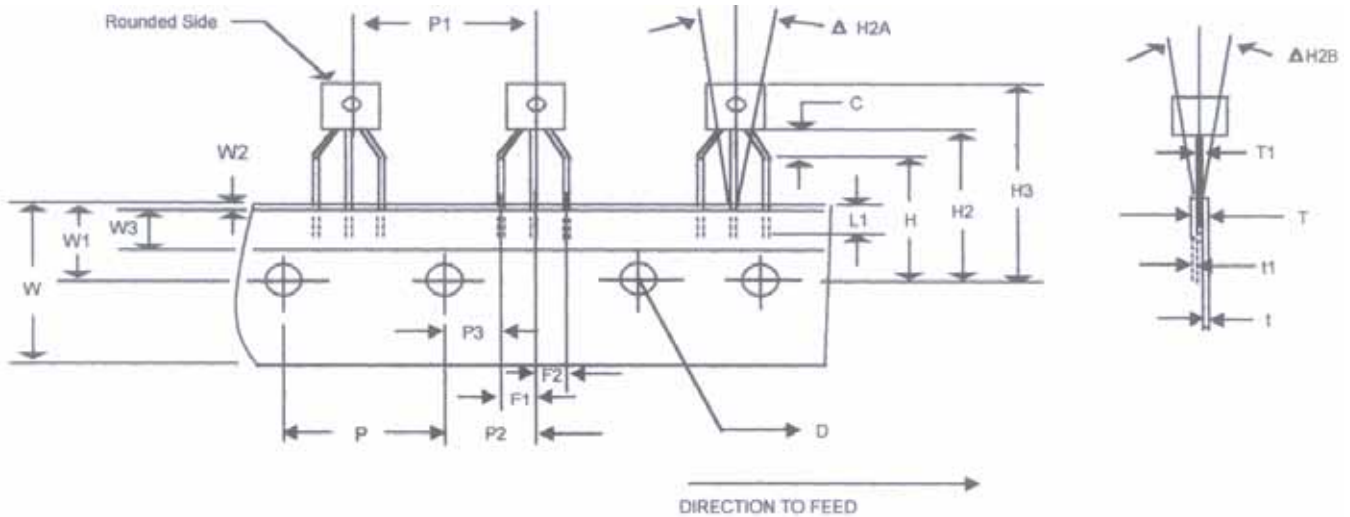


| SYM | DIMENSION IN INCHES |       |       | DIMENSION IN MM |      |      |
|-----|---------------------|-------|-------|-----------------|------|------|
|     | MIN                 | NOM   | MAX   | MIN             | NOM  | MAX  |
| A   | 0.059               | 0.062 | 0.065 | 1.50            | 1.57 | 1.65 |
| A1  | 0.004               | 0.008 | 0.010 | 0.10            | 0.20 | 0.25 |
| A2  | 0.051               | 0.054 | 0.057 | 1.30            | 1.37 | 1.45 |
| b   | 0.013               | 0.016 | 0.020 | 0.33            | 0.41 | 0.51 |
| c   | 0.007               | 0.008 | 0.010 | 0.18            | 0.20 | 0.25 |
| D   | 0.191               | 0.193 | 0.195 | 4.85            | 4.90 | 4.95 |
| E1  | 0.151               | 0.153 | 0.155 | 3.84            | 3.89 | 3.94 |
| E   | 0.228               | 0.234 | 0.240 | 5.79            | 5.94 | 6.10 |
| e   | 0.050               |       |       | 1.27            |      |      |
| L   | 0.020               | 0.024 | 0.032 | 0.51            | 0.61 | 0.81 |
| L1  | 0.039               | 0.041 | 0.043 | 0.99            | 1.04 | 1.09 |
| Ø   | 0*                  | -     | B*    | 0*              | -    | B*   |
| h   | 0.011               | 0.015 | 0.019 | 0.28            | 0.38 | 0.48 |

**NOTES:**  
1. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
2. COPLANARITY APPLIES TO THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.003" [0.08 mm].  
3. BASED FROM JEDEC NS-012 VARIATION AA.



TO-92 AMMO PACK SPECIFICATIONS

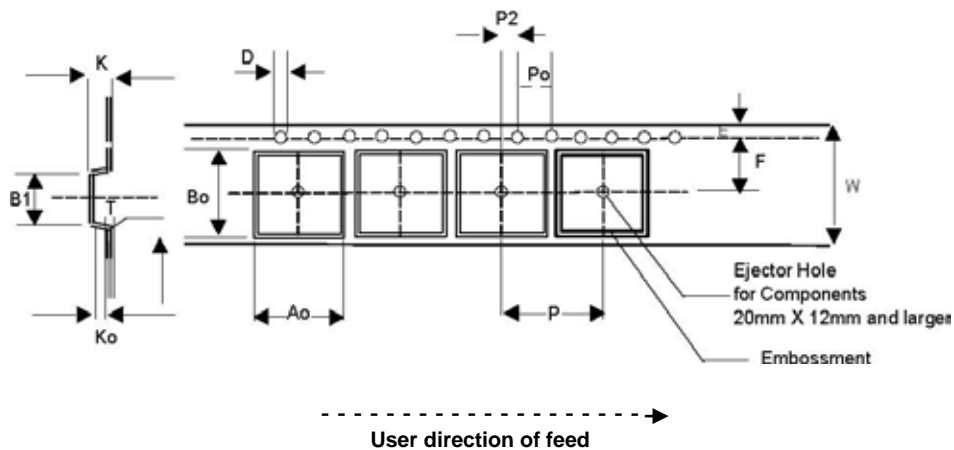


| SYMBOL      | DESCRIPTION                                   | NOMINAL VALUE |       | TOLERANCES |       |       |       |
|-------------|---|---------------|-------|------------|-------|-------|-------|
|             |   | mm            | inch  | min        |       | max   |       |
| D           | Feed Hole Diameter                            | 4.0           | 0.157 | 3.8        | 0.150 | 4.2   | 0.165 |
| T1 (POD)    | Component Lead Thickness                      | 0.405         | 0.016 | 0.36       | 0.014 | 0.45  | 0.018 |
| F1/F2       | Lead Pitch (Left / Right)                     | 2.54          | 0.100 | 2.4        | 0.094 | 2.8   | 0.110 |
| C           | Bottom of Component to Seating Plane          | 2.50          | 0.098 | 1.50       | 0.059 | 4.00  | 0.157 |
| W1          | Edge to Sprocket Hole Center                  | 9.0           | 0.354 | 8.50       | 0.335 | 9.50  | 0.374 |
| H2A         | Deflection (Left or Right)                    | 0.50          | 0.020 | 0          | 0     | 0.50  | 0.020 |
| H2B         | Deflection (Front or Rear)                    | 1.0           | 0.039 | 0          | 0     | 1.0   | 0.039 |
| H2 (H + C)  | Feed Hole to Bottom of Component              | 18.5          | 0.728 | 17.00      | 0.669 | 20.50 | 0.087 |
| H           | Height of Seating Plane                       | 16            | 0.630 | 15.5       | 0.610 | 16.5  | 0.650 |
| H3          | Feed Hole Center to Overall Transistor Height | 27.75         | 1.092 | 23.5       | 0.925 | 32.0  | 1.260 |
| L           | Defective Unit Clipped Dimension              | -             | -     | -          | -     | 11.0  | 0.433 |
| L1          | Leadwire Enclosure                            | 2.50          | 0.098 | 2.50       | 0.098 | -     | -     |
| P           | Feed Hole Pitch                               | 12.7          | 0.500 | 12.40      | 0.488 | 13.0  | 0.512 |
| P2          | Center of Feed Hole to Center Lead            | 6.35          | 0.250 | 6.0        | 0.234 | 6.75  | 0.266 |
| P3 (P2-F1)  | First Lead Spacing Dimension                  | 3.75          | 0.148 | 3.6        | 0.142 | 3.95  | 0.156 |
| P1          | Center Lead to Center Lead                    | 12.7          | 0.500 | 12.2       | 0.500 | 13.2  | 0.520 |
| t1          | Adhesive Tape Thickness                       | 0.18          | 0.007 | 0.16       | 0.006 | 0.20  | 0.008 |
| T (t+t1+T1) | Overall Taped Package Thickness               | -             | -     | -          | -     | 1.55  | 0.061 |
| T           | Carrier Strip Thickness                       | 0.37          | 0.015 | 0.27       | 0.011 | 0.47  | 0.018 |
| W           | Carrier Strip Width (18mm)                    | 18.00         | 0.709 | 17.5       | 0.689 | 19.0  | 0.748 |
| W3          | Adhesive Tape Width (6mm)                     | 6.00          | 0.236 | 5.5        | 0.217 | 6.3   | 0.248 |
| W2          | Adhesive Tape Position                        | 0.25          | 0.010 | 0          | 0     | 0.50  | 0.020 |

| TO-92 Ammo Pack Requirement |    |                   |              |
|-----------------------------|----|-------------------|--------------|
| Components                  |    | Tape Width (W) mm | Fan Fold Box |
| TO92                        | 3L | 18                | 2000         |

**PACKAGE MECHANICAL DRAWING**

**Surface Mountable Tape & Reel Specifications in mm (inch)  
(SOIC, SOT-23 and SOT-89)**

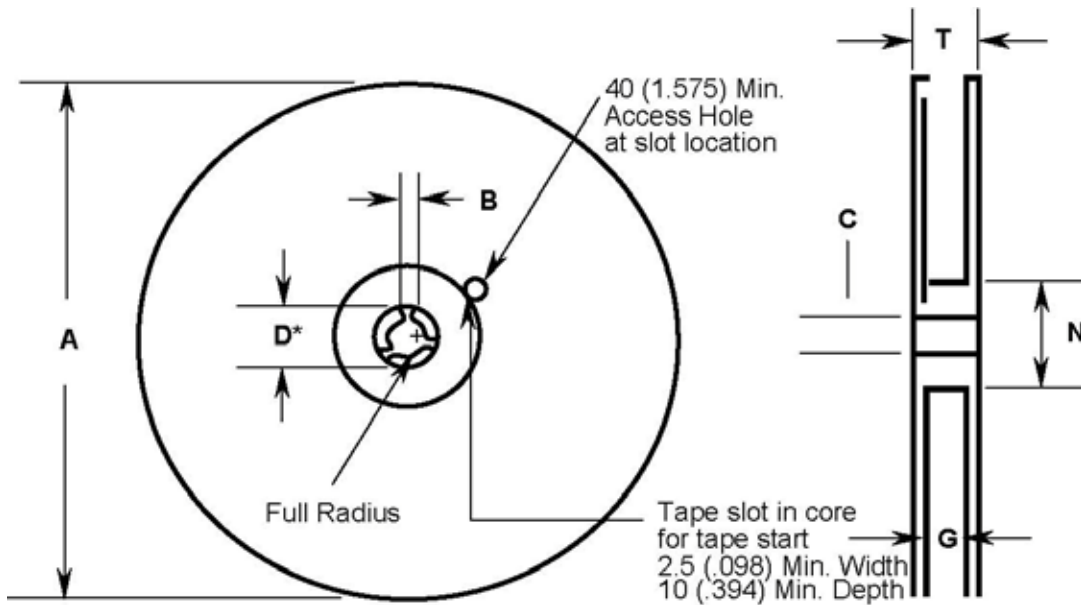


| Tape Size (W)   | D                        | E                        | P0                      | T (Max)         | A0, B0, K0 | T1 (Max)        | Constant Dimensions |
|-----------------|--------------------------|--------------------------|-------------------------|-----------------|------------|-----------------|---------------------|
| 8, 12, 16, 24mm | 1.55±0.05<br>(.061±.002) | 1.75±0.10<br>(.069±.004) | 4.0±0.10<br>(.157±.004) | 0.400<br>(.016) | See Note   | 0.100<br>(.004) |                     |

| Tape Size (W) | B1 Max.       | D1 Min.       | F                       | K Max.        | P2        |                     |
|---------------|---------------|---------------|-------------------------|---------------|-----------|---------------------|
| 8 mm          | 4.2<br>(.165) | 1.0<br>(.039) | 3.5±0.05<br>(.138±.002) | 2.4<br>(.094) | 2.0±.05   |                     |
| 12 mm         | 8.2<br>(.323) | 1.5<br>(.059) | 5.5±0.05<br>(.217±.002) | 4.5<br>(.177) | .079±.002 | Variable Dimensions |

| Per Package Requirement |    |                   |                     |                  |          |
|-------------------------|----|-------------------|---------------------|------------------|----------|
| Components              |    | Tape Width (W) mm | Cavity Pitch (P) mm | Devices per Reel |          |
|                         |    |                   |                     | 7" Reel          | 13" Reel |
| SOIC                    | 8L | 12                | 8                   | -                | 2500     |
| SOT-23                  | 3L | 8                 | 4                   | 3000             | -        |
| SOT-23                  | 5L | 8                 | 4                   | 3000             | -        |
| SOT-89                  | 3L | 12                | 8                   | -                | 2500     |

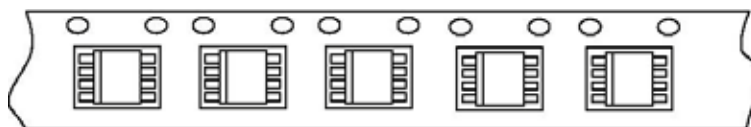
**Note:** A0 B0 K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 [.002] min. to 0.50 [.020] max. for 8mm tape, 0.05 [.002] min to 0.65 [.026] max for 12mm tape.



| REEL DIMENSIONS |                 |               |                          |                |               |                                       |                |
|-----------------|-----------------|---------------|--------------------------|----------------|---------------|---------------------------------------|----------------|
| Tape Size       | A<br>Max.       | B<br>Min.     | C                        | D*<br>Min.     | N<br>Min.     | G                                     | T<br>Max.      |
| 8mm             | 330<br>(12.992) | 1.5<br>(.059) | 13.0±0.20<br>(.152±.008) | 20.2<br>(.795) | 50<br>(1.973) | 8.4±1.5<br>0.0<br>(.331±.059)<br>0.0  | 14.4<br>(.567) |
| 12mm            | 330<br>(12.992) | 1.5<br>(.059) | 13.0±0.20<br>(.152±.008) | 20.2<br>(.795) | 50<br>(1.973) | 12.4±2.0<br>0.0<br>(.488±.078)<br>0.0 | 14.4<br>(.567) |

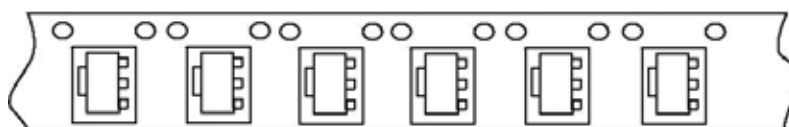
**MECHANICAL POLARIZATION**

**SOIC-8L DEVICE**



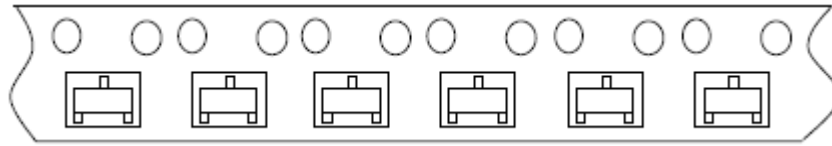
User direction of feed ----->

**SOT-89 DEVICE**



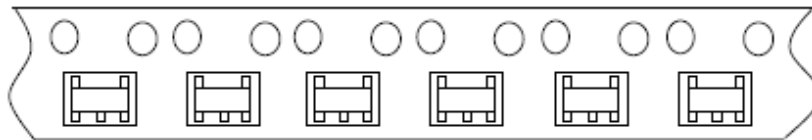
User direction of feed ----->

**SOT-23 3L DEVICE**



User direction of feed ----->

**SOT-23 5L DEVICE**



User direction of feed ----->